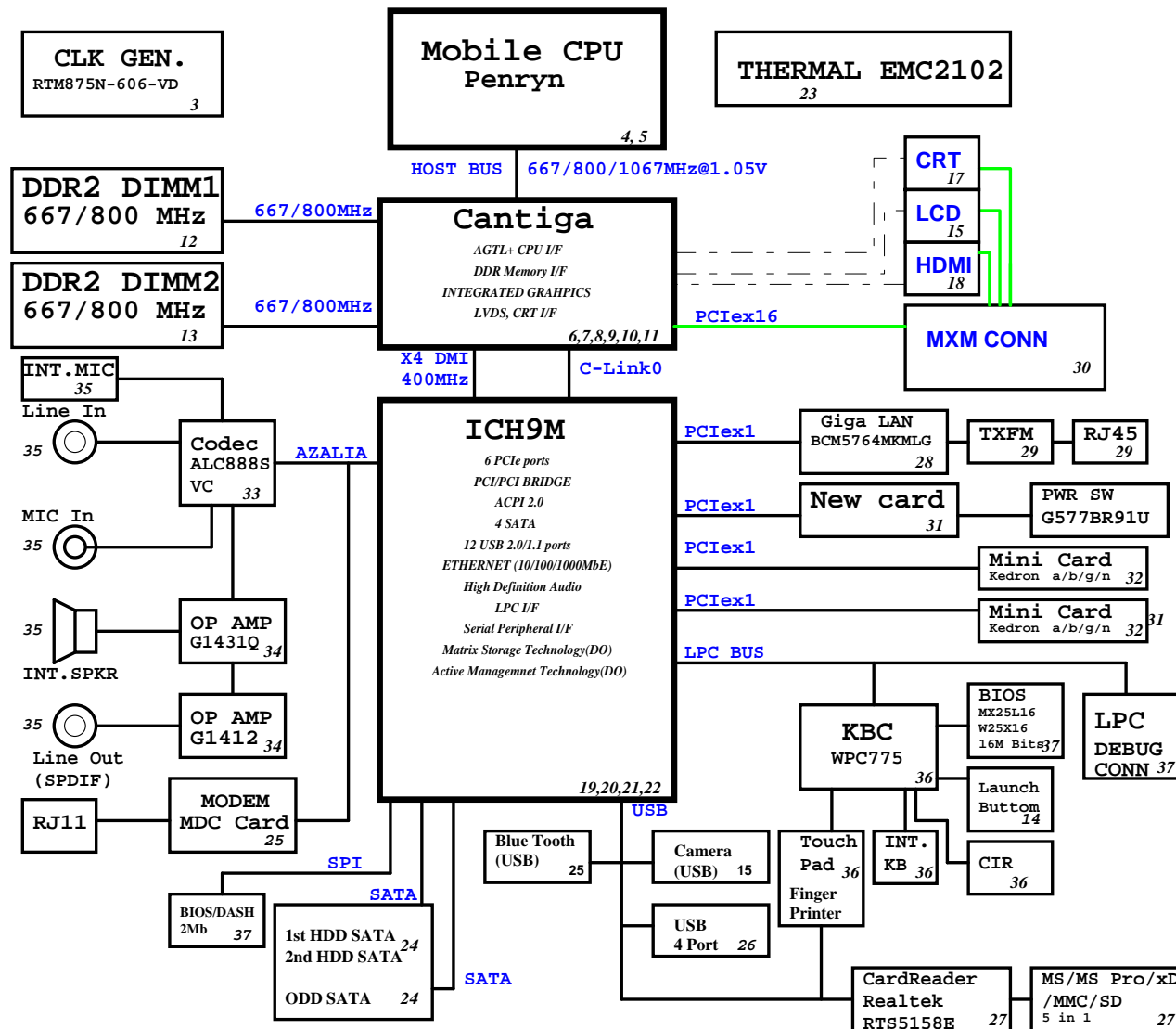


Big Bear 2 Block Diagram

Project code: 91.4AV01.001
PCB P/N : 48.4AV01.
REVISION : -1



PCB STACKUP

TOP	_____
VCC	_____
S	_____
S	_____
GND	_____
BOTTOM	_____

SYSTEM DC/DC	
TPS51125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
SYSTEM DC/DC	
TPS51124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
RT9026 44	
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3
RT9018A 44	
1D8V_S3	1D5V_S0
G9131 44	
3D3V_S0	2D5V_S0
GFXCORE DC/DC	
ISL6263 46	
INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7-1.25V
CPU DC/DC	
ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35-1.5V
CHARGER	
BQ24745 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
BLOCK DIAGRAM			
Size	Document Number		Rev
Custom	Big Bear 2		-1
Date: Wednesday, October 22, 2008		Sheet 1 of	50

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

PCIE Routing

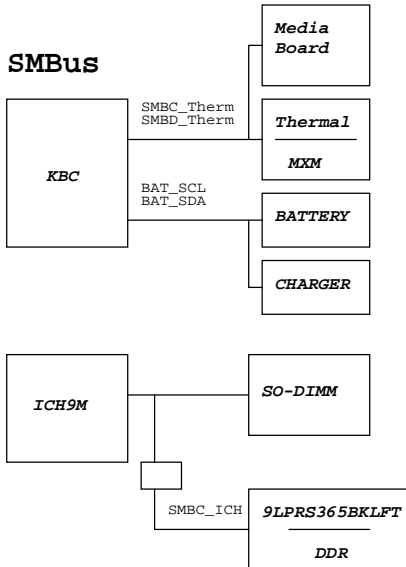
LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN/TV
LANE4	JMB385 Card Reader
LANE5	NewCard
LANE6	NC

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USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	USB5(DOCK)
4	USB3
5	Bluetooth
6	FP
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC

SMBus



ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS1PVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

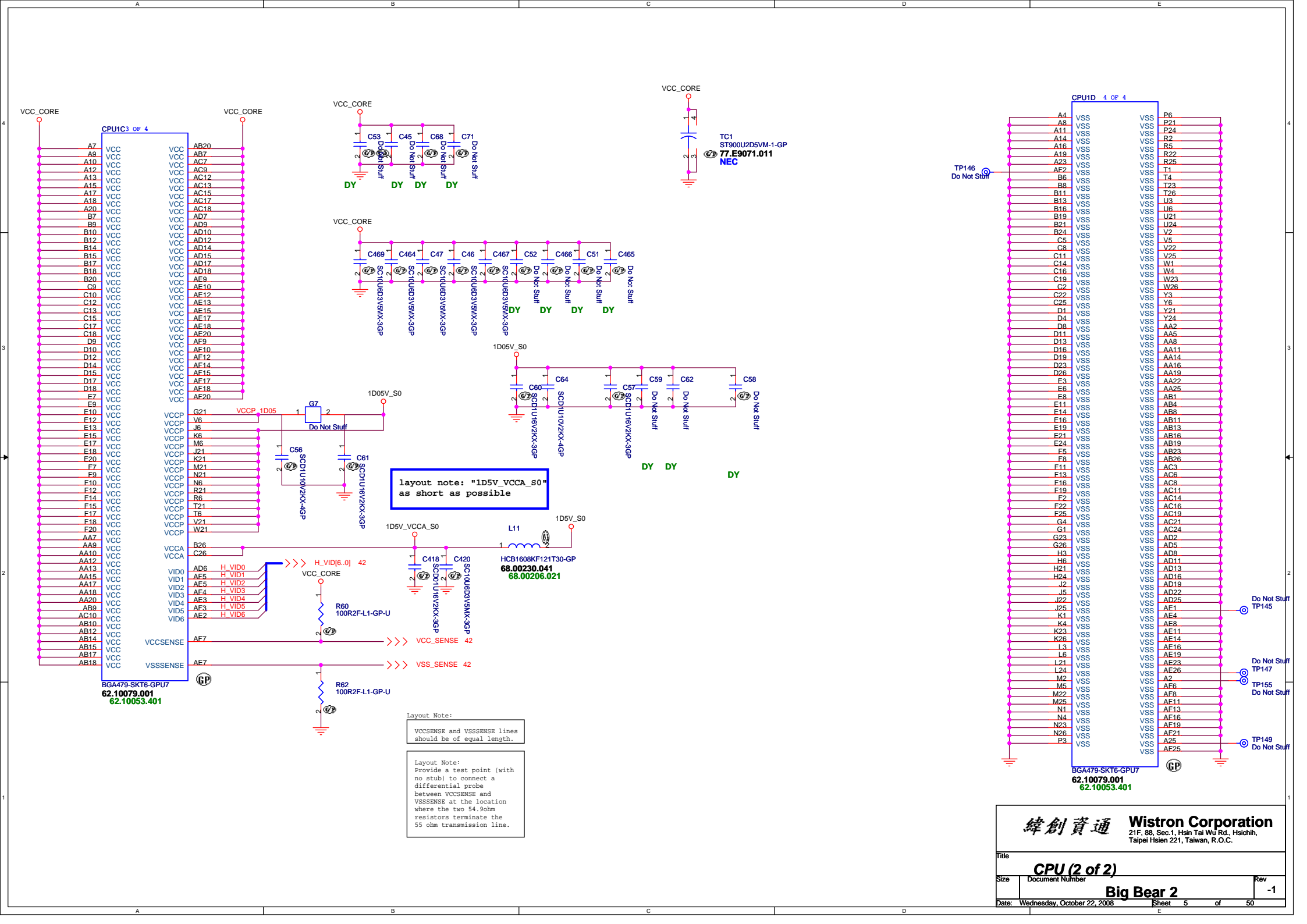
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default). 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

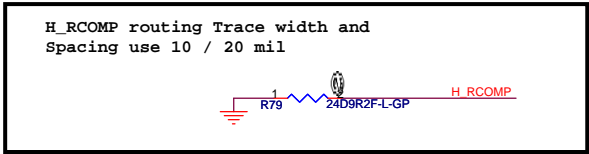
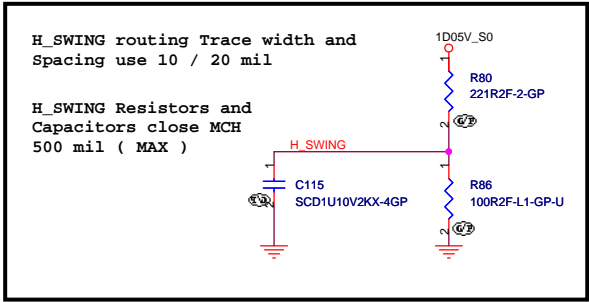
NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

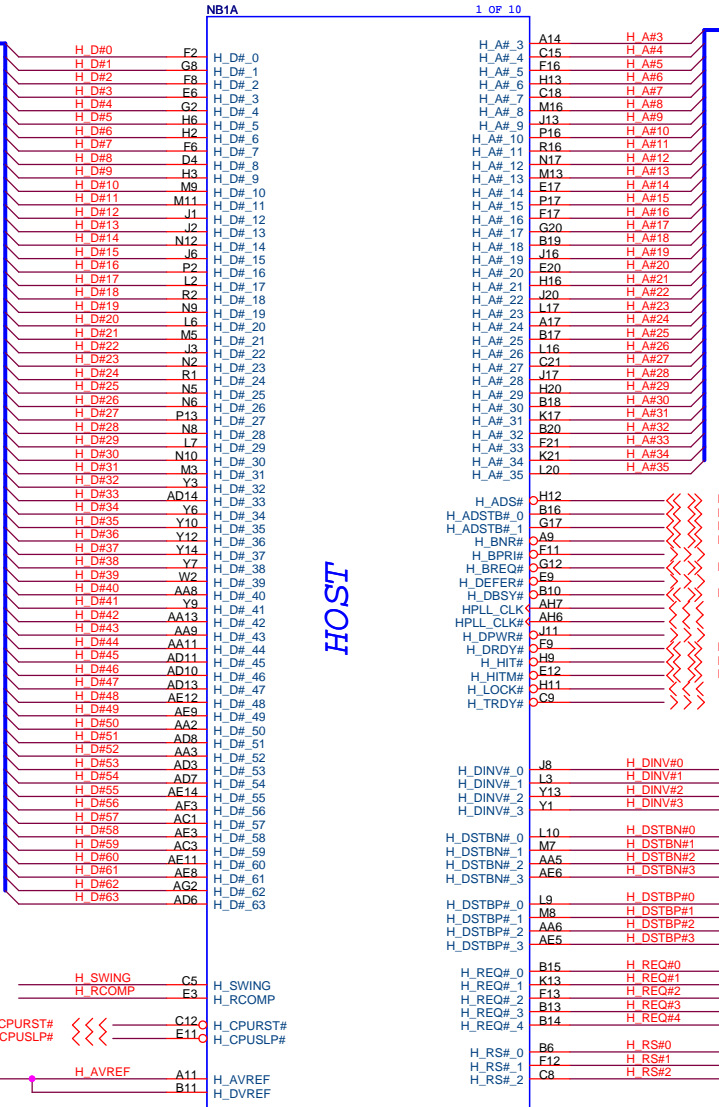
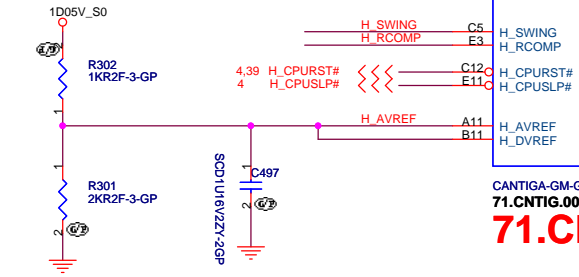
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Title		Reference	
Size A3	Document Number	Rev -1	
Date: Wednesday, October 22, 2008	Sheet 2 of 50	Big Bear 2	

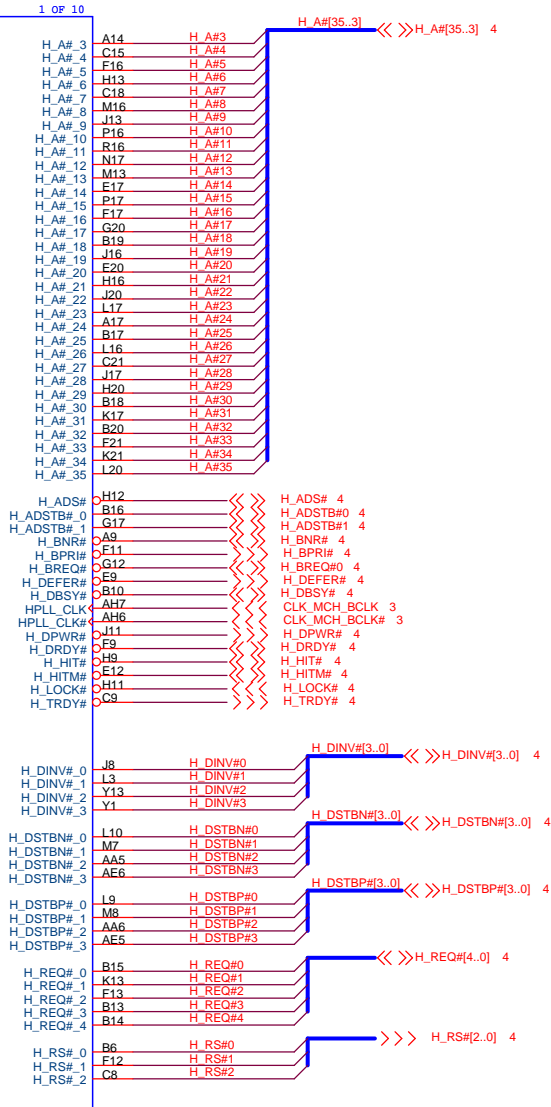


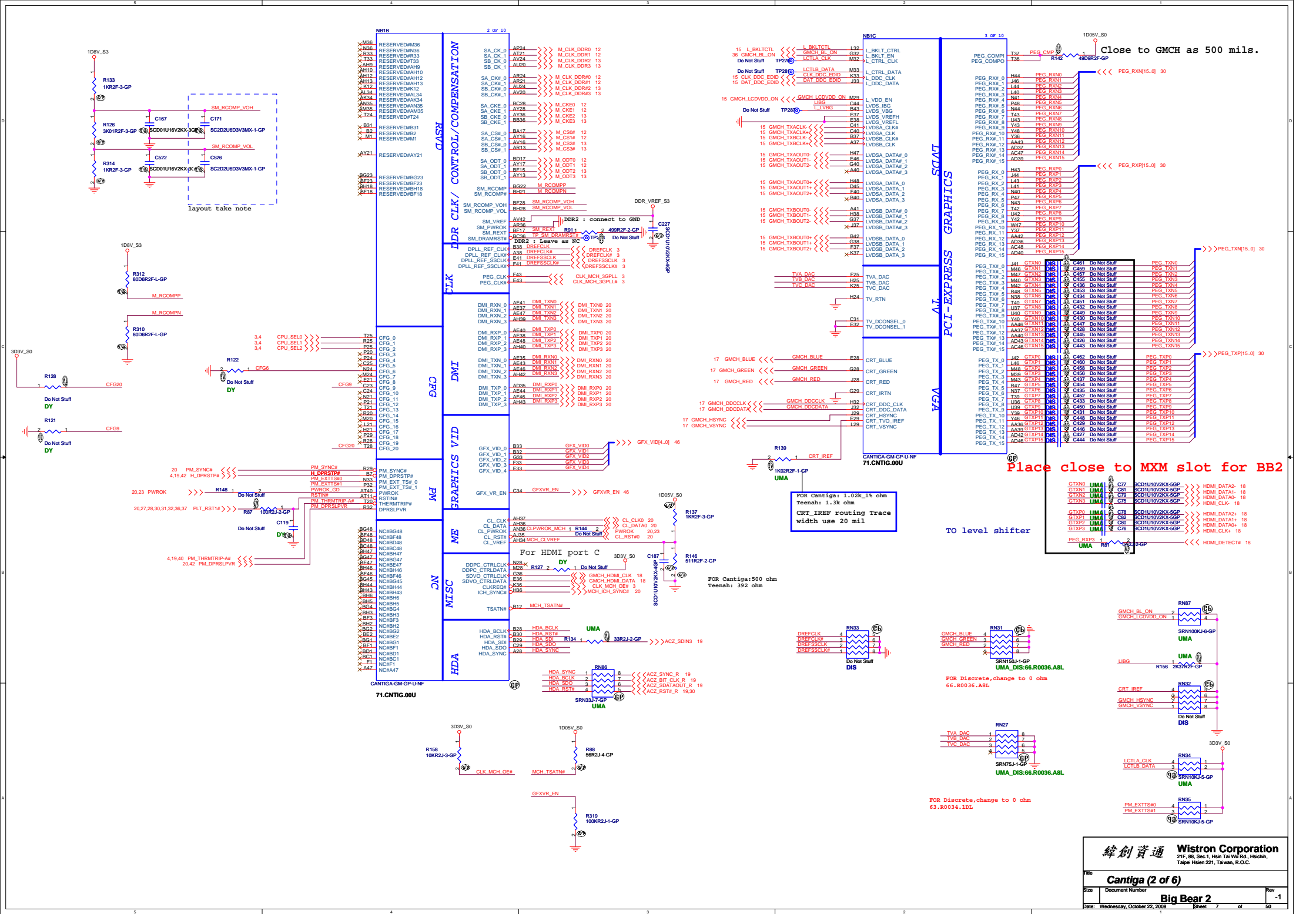


Place them near to the chip (< 0.5")



HOST





12 M_A_DQ[63.0] <<< M_A_DQ[63.0]

M A DQ0 AJ38 SA_DQ_0

M A DQ1 AJ41 SA_DQ_1

M A DQ2 AN38 SA_DQ_2

M A DQ3 AM38 SA_DQ_3

M A DQ4 AJ36 SA_DQ_4

M A DQ5 AJ40 SA_DQ_5

M A DQ6 AM44 SA_DQ_6

M A DQ7 AM42 SA_DQ_7

M A DQ8 AN43 SA_DQ_8

M A DQ9 AN44 SA_DQ_9

M A DQ10 AU40 SA_DQ_10

M A DQ11 AT38 SA_DQ_11

M A DQ12 AN41 SA_DQ_12

M A DQ13 AN39 SA_DQ_13

M A DQ14 AU44 SA_DQ_14

M A DQ15 AU42 SA_DQ_15

M A DQ16 AV39 SA_DQ_16

M A DQ17 AV44 SA_DQ_17

M A DQ18 BA40 SA_DQ_18

M A DQ19 BD43 SA_DQ_19

M A DQ20 AV41 SA_DQ_20

M A DQ21 AY43 SA_DQ_21

M A DQ22 BB41 SA_DQ_22

M A DQ23 BC40 SA_DQ_23

M A DQ24 AV37 SA_DQ_24

M A DQ25 BD38 SA_DQ_25

M A DQ26 AV37 SA_DQ_26

M A DQ27 AT36 SA_DQ_27

M A DQ28 AY38 SA_DQ_28

M A DQ29 BB38 SA_DQ_29

M A DQ30 AV36 SA_DQ_30

M A DQ31 AW36 SA_DQ_31

M A DQ32 BD13 SA_DQ_32

M A DQ33 AU11 SA_DQ_33

M A DQ34 BC11 SA_DQ_34

M A DQ35 BA12 SA_DQ_35

M A DQ36 AU13 SA_DQ_36

M A DQ37 AV13 SA_DQ_37

M A DQ38 BD12 SA_DQ_38

M A DQ39 BC12 SA_DQ_39

M A DQ40 BB9 SA_DQ_40

M A DQ41 BA9 SA_DQ_41

M A DQ42 AU10 SA_DQ_42

M A DQ43 AV9 SA_DQ_43

M A DQ44 BA11 SA_DQ_44

M A DQ45 BD9 SA_DQ_45

M A DQ46 AY8 SA_DQ_46

M A DQ47 BA6 SA_DQ_47

M A DQ48 AV5 SA_DQ_48

M A DQ49 AV7 SA_DQ_49

M A DQ50 AT9 SA_DQ_50

M A DQ51 AN8 SA_DQ_51

M A DQ52 AU5 SA_DQ_52

M A DQ53 AU6 SA_DQ_53

M A DQ54 AT5 SA_DQ_54

M A DQ55 AN10 SA_DQ_55

M A DQ56 AM11 SA_DQ_56

M A DQ57 AM5 SA_DQ_57

M A DQ58 AJ9 SA_DQ_58

M A DQ59 AJ8 SA_DQ_59

M A DQ60 AN12 SA_DQ_60

M A DQ61 AM13 SA_DQ_61

M A DQ62 AJ11 SA_DQ_62

M A DQ63 AJ12 SA_DQ_63

NB1D

4 OF 10

SA_BS_0 BD21

SA_BS_1 BG18

SA_BS_2 AT25

SA_RAS# BB20

SA_CAS# BD20

SA_WE# AY20

SA_DM_0 AM37

SA_DM_1 AT41

SA_DM_2 AY41

SA_DM_3 AU39

SA_DM_4 BB12

SA_DM_5 AY6

SA_DM_6 AT7

SA_DM_7 AJ5

SA_DQS_0 AJ44

SA_DQS_1 AT44

SA_DQS_2 BA43

SA_DQS_3 BC37

SA_DQS_4 AW12

SA_DQS_5 BC8

SA_DQS_6 AU8

SA_DQS_7 AM7

SA_DQS#_0 AJ43

SA_DQS#_1 AT43

SA_DQS#_2 BA44

SA_DQS#_3 BD37

SA_DQS#_4 AY12

SA_DQS#_5 BD8

SA_DQS#_6 AU9

SA_DQS#_7 AM8

SA_MA_0 BA21

SA_MA_1 BC24

SA_MA_2 BG24

SA_MA_3 BH24

SA_MA_4 BG25

SA_MA_5 BA24

SA_MA_6 BD24

SA_MA_7 BG27

SA_MA_8 BF25

SA_MA_9 AW24

SA_MA_10 BC21

SA_MA_11 BG26

SA_MA_12 BH17

SA_MA_13 AY25

SA_MA_14



CANTIGA-GM-GP-U-NF
71.CNTIG.00U

13 M_B_DQ[63.0] <<< M_B_DQ[63.0]

M B DQ0 AK47 SB_DQ_0

M B DQ1 AH46 SB_DQ_1

M B DQ2 AP47 SB_DQ_2

M B DQ3 AP46 SB_DQ_3

M B DQ4 AJ46 SB_DQ_4

M B DQ5 AJ48 SB_DQ_5

M B DQ6 AM48 SB_DQ_6

M B DQ7 AP48 SB_DQ_7

M B DQ8 AU47 SB_DQ_8

M B DQ9 BA46 SB_DQ_9

M B DQ10 BA48 SB_DQ_10

M B DQ11 AY48 SB_DQ_11

M B DQ12 AT47 SB_DQ_12

M B DQ13 AR47 SB_DQ_13

M B DQ14 BA47 SB_DQ_14

M B DQ15 BC47 SB_DQ_15

M B DQ16 BC46 SB_DQ_16

M B DQ17 BC44 SB_DQ_17

M B DQ18 BG43 SB_DQ_18

M B DQ19 BF43 SB_DQ_19

M B DQ20 BF45 SB_DQ_20

M B DQ21 BC41 SB_DQ_21

M B DQ22 BF40 SB_DQ_22

M B DQ23 BF41 SB_DQ_23

M B DQ24 BG38 SB_DQ_24

M B DQ25 BF38 SB_DQ_25

M B DQ26 BH35 SB_DQ_26

M B DQ27 BC35 SB_DQ_27

M B DQ28 BH40 SB_DQ_28

M B DQ29 BC38 SB_DQ_29

M B DQ30 BG34 SB_DQ_30

M B DQ31 BH34 SB_DQ_31

M B DQ32 BH14 SB_DQ_32

M B DQ33 BG12 SB_DQ_33

M B DQ34 BH11 SB_DQ_34

M B DQ35 BG8 SB_DQ_35

M B DQ36 BH12 SB_DQ_36

M B DQ37 BF11 SB_DQ_37

M B DQ38 BF8 SB_DQ_38

M B DQ39 BG7 SB_DQ_39

M B DQ40 BC5 SB_DQ_40

M B DQ41 BC6 SB_DQ_41

M B DQ42 AY1 SB_DQ_42

M B DQ43 AY1 SB_DQ_43

M B DQ44 BF6 SB_DQ_44

M B DQ45 BF5 SB_DQ_45

M B DQ46 BA1 SB_DQ_46

M B DQ47 BD3 SB_DQ_47

M B DQ48 AV2 SB_DQ_48

M B DQ49 AU3 SB_DQ_49

M B DQ50 AR3 SB_DQ_50

M B DQ51 AN2 SB_DQ_51

M B DQ52 AY2 SB_DQ_52

M B DQ53 AV1 SB_DQ_53

M B DQ54 AP3 SB_DQ_54

M B DQ55 AR1 SB_DQ_55

M B DQ56 AL1 SB_DQ_56

M B DQ57 AL2 SB_DQ_57

M B DQ58 AJ1 SB_DQ_58

M B DQ59 AH1 SB_DQ_59

M B DQ60 AM2 SB_DQ_60

M B DQ61 AM3 SB_DQ_61

M B DQ62 AH3 SB_DQ_62

M B DQ63 AJ5 SB_DQ_63

NB1E

5 OF 10

SB_BS_0 BC16

SB_BS_1 BB17

SB_BS_2 BB33

SB_RAS# AU17

SB_CAS# BG16

SB_WE# BF14

SB_DM_0 AM47

SB_DM_1 AY47

SB_DM_2 BD40

SB_DM_3 BF35

SB_DM_4 BG11

SB_DM_5 BA3

SB_DM_6 AP1

SB_DM_7 AK2

SB_DQS_0 AL47

SB_DQS_1 AV48

SB_DQS_2 BG41

SB_DQS_3 BG37

SB_DQS_4 BH9

SB_DQS_5 BB2

SB_DQS_6 AU1

SB_DQS_7 AN6

SB_DQS#_0 AL46

SB_DQS#_1 AV47

SB_DQS#_2 BH41

SB_DQS#_3 BH37

SB_DQS#_4 BG9

SB_DQS#_5 BC2

SB_DQS#_6 AT2

SB_DQS#_7 AN5

SB_MA_0 AV17

SB_MA_1 BA25

SB_MA_2 BC25

SB_MA_3 AU25

SB_MA_4 AW25

SB_MA_5 BB28

SB_MA_6 AU28

SB_MA_7 AW28

SB_MA_8 AT33

SB_MA_9 BD33

SB_MA_10 BB16

SB_MA_11 AW33

SB_MA_12 AY33

SB_MA_13 BH15

SB_MA_14 AU33



CANTIGA-GM-GP-U-NF
71.CNTIG.00U

DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

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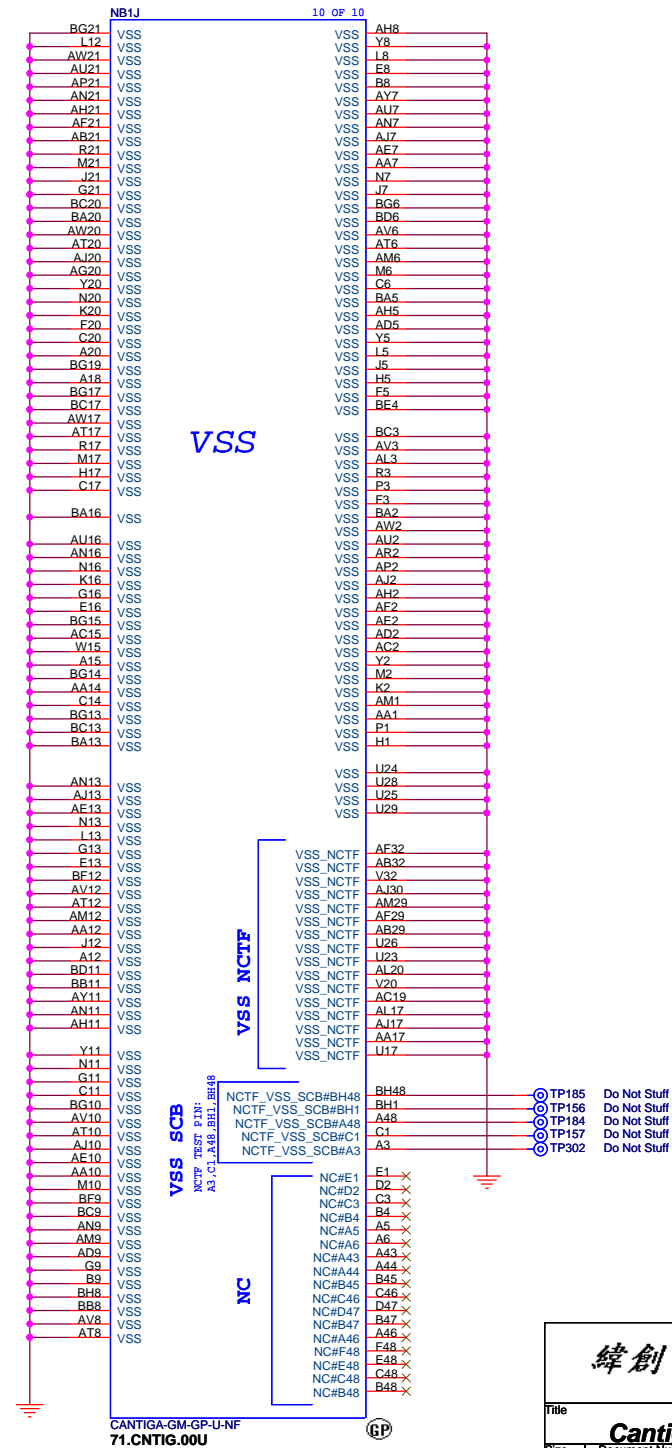
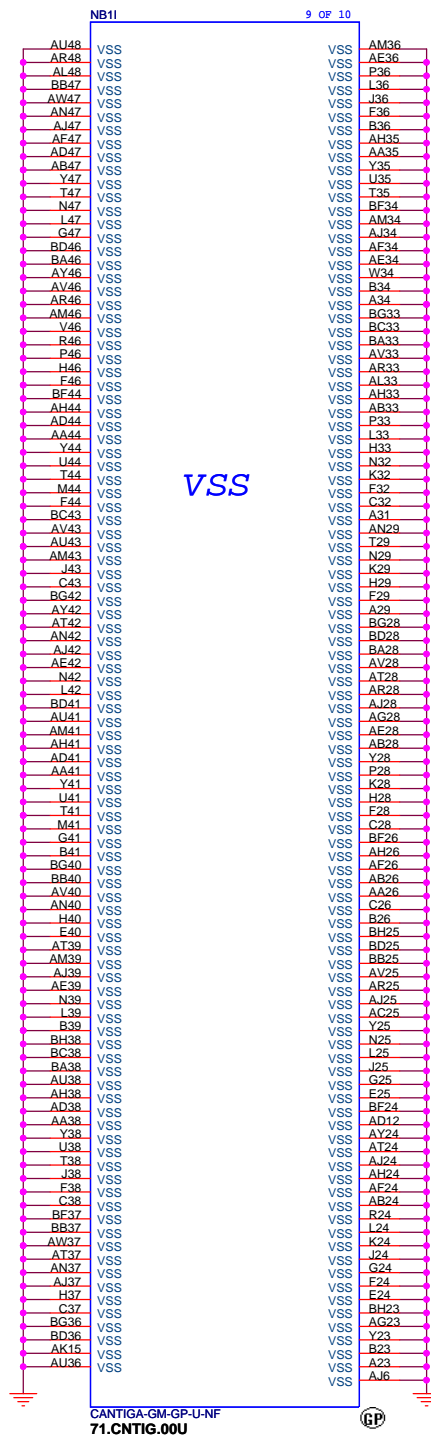
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Size Document Number Rev
Date: Wednesday, October 22, 2008 Sheet 8 of 50

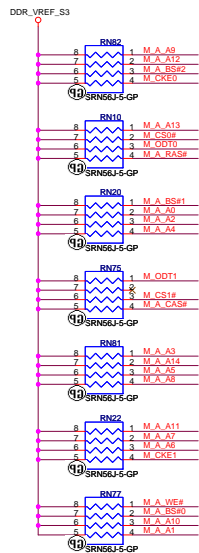
Cantiga (3 of 6)

Big Bear 2

-1

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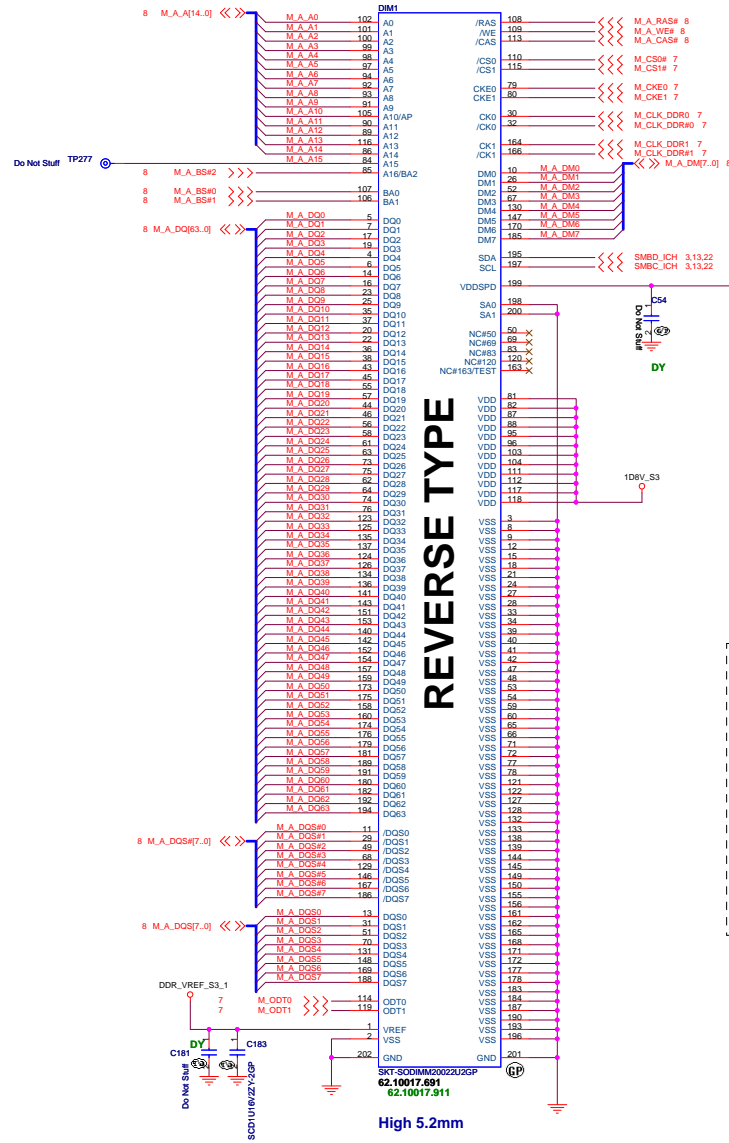
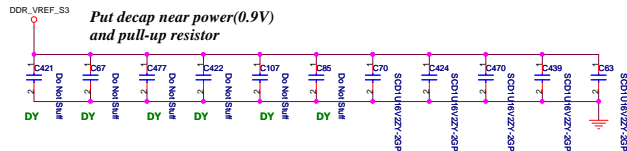


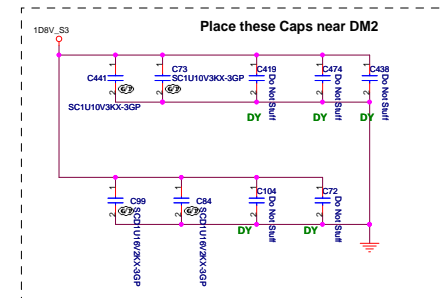
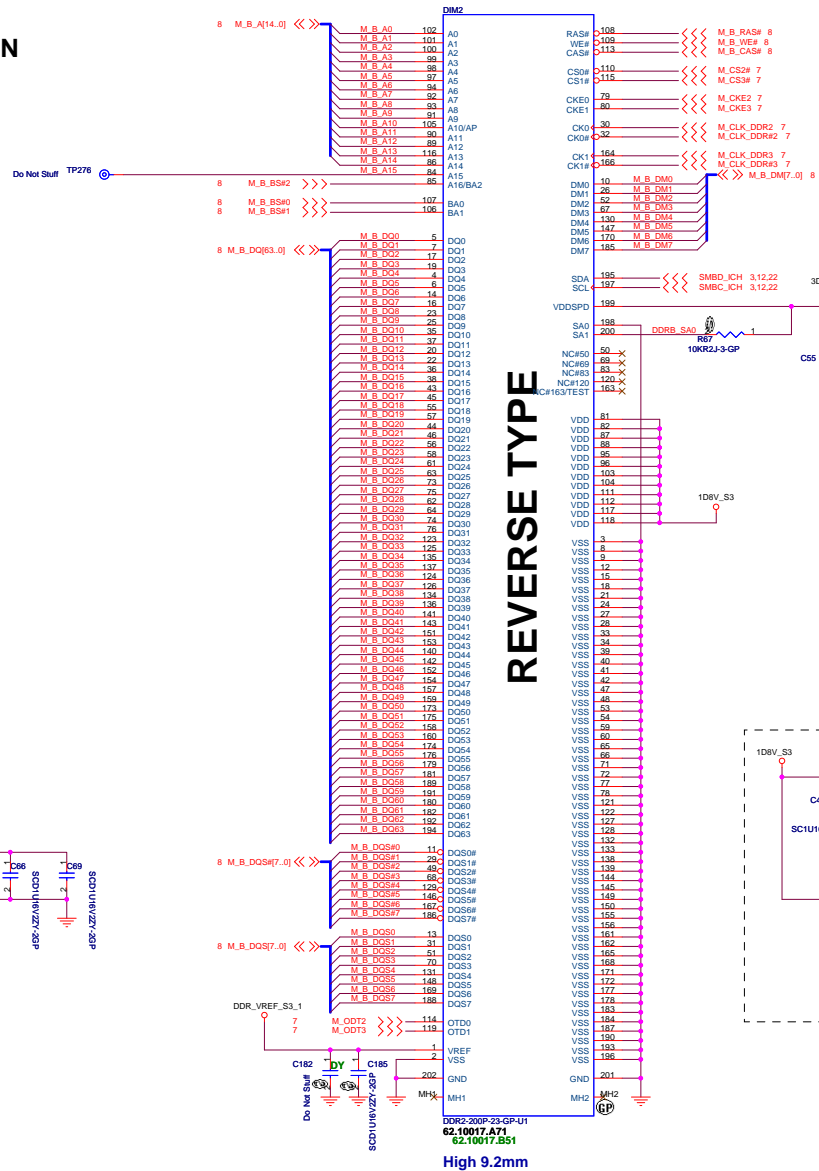
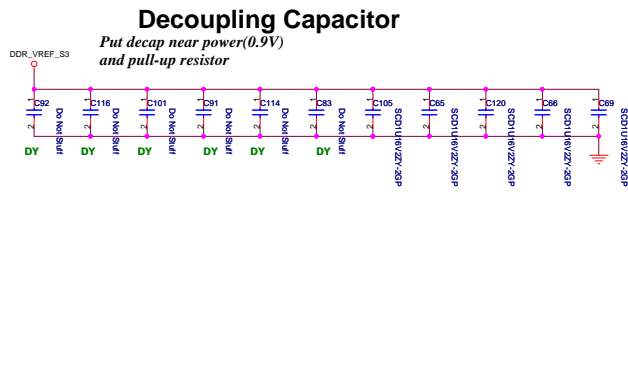
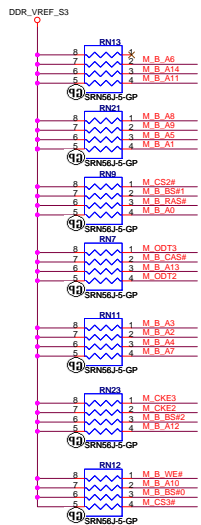


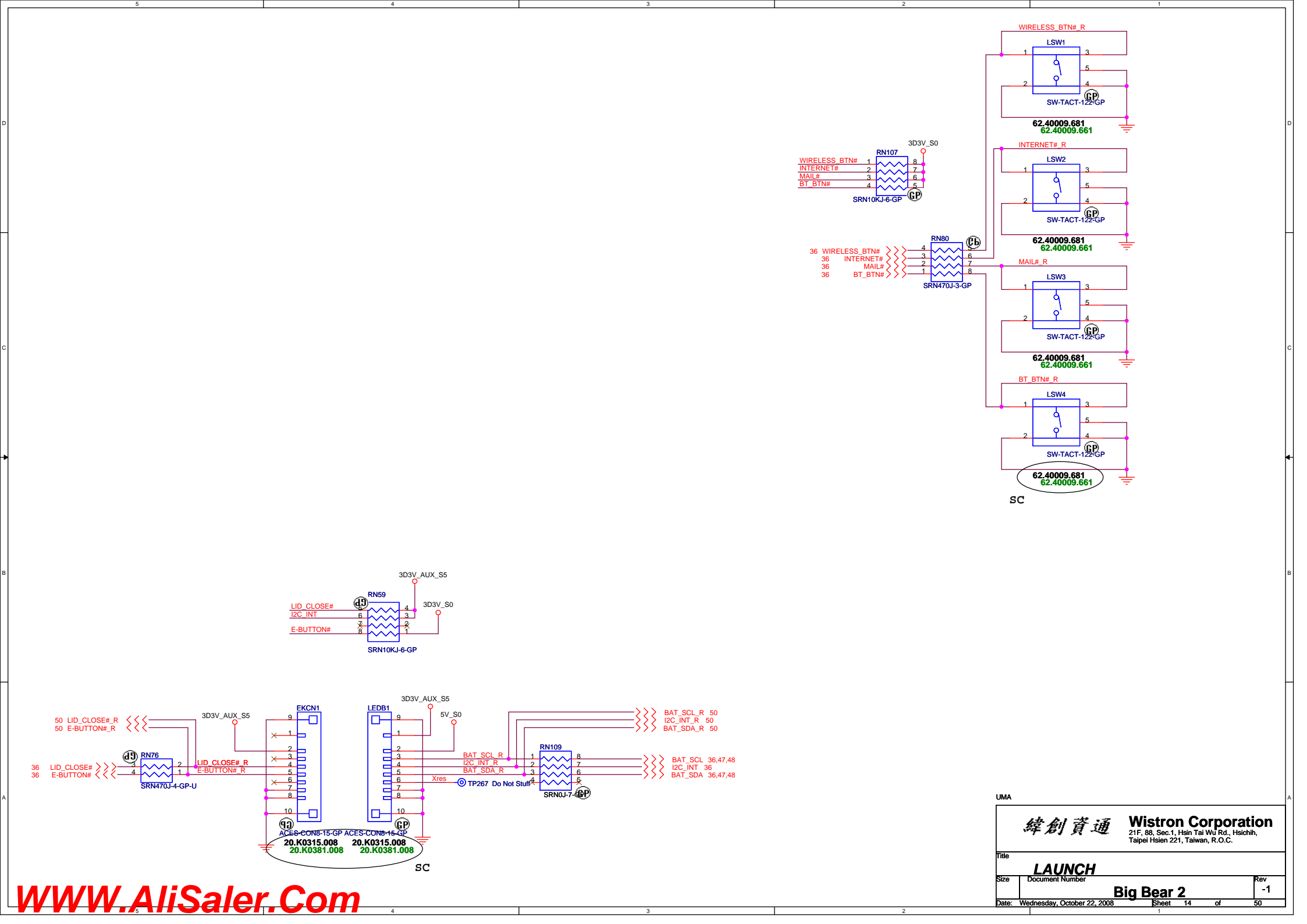
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

Decoupling Capacitor

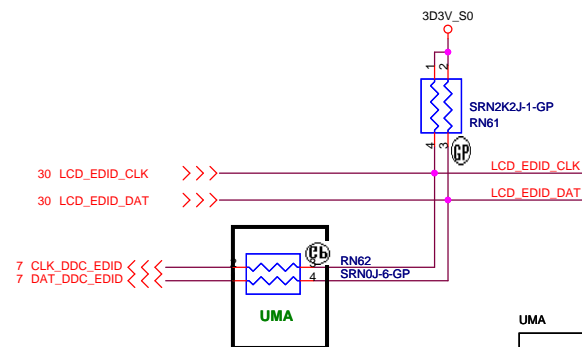
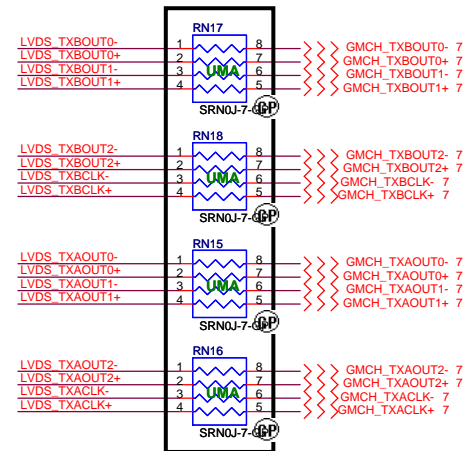
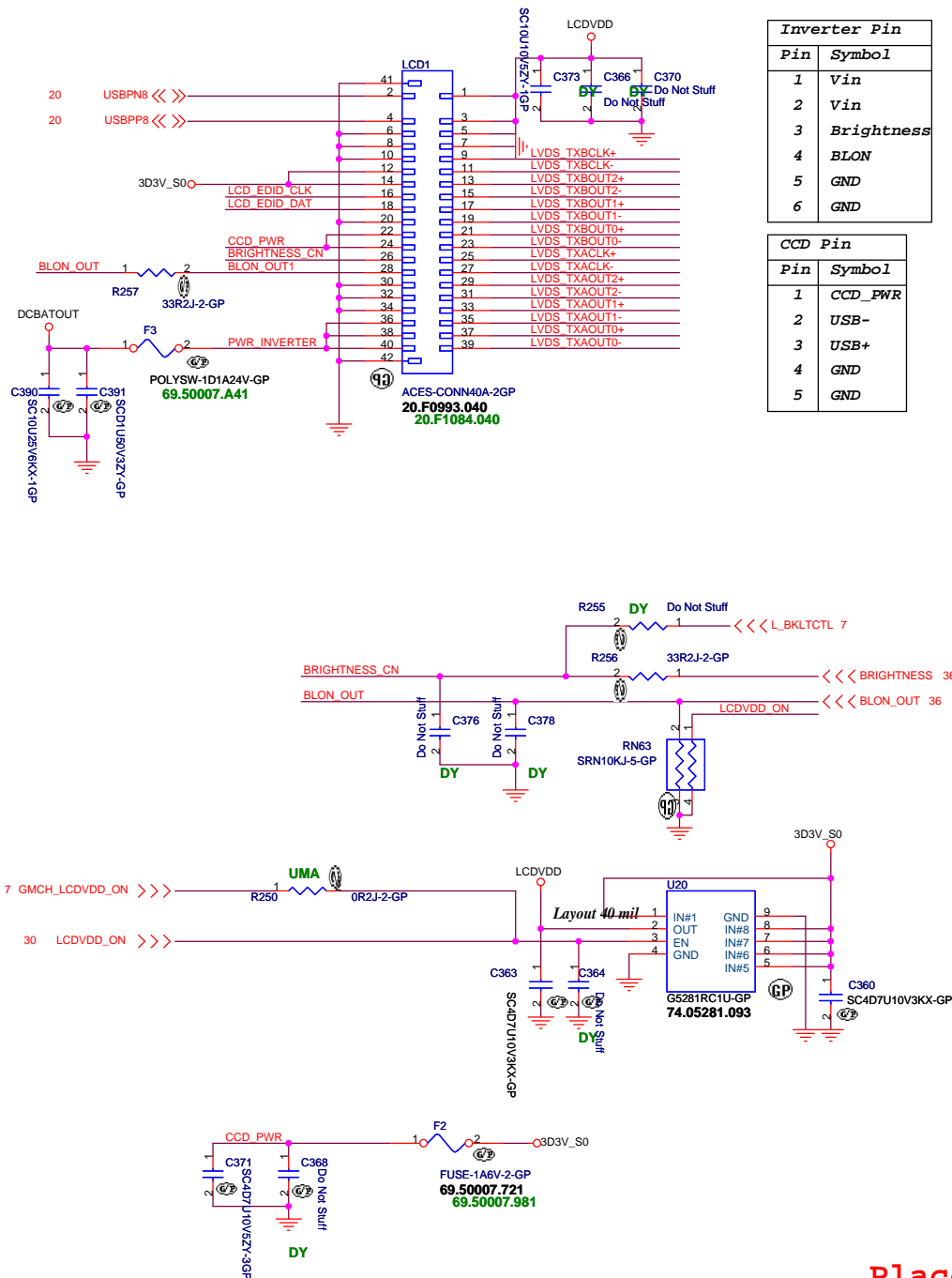




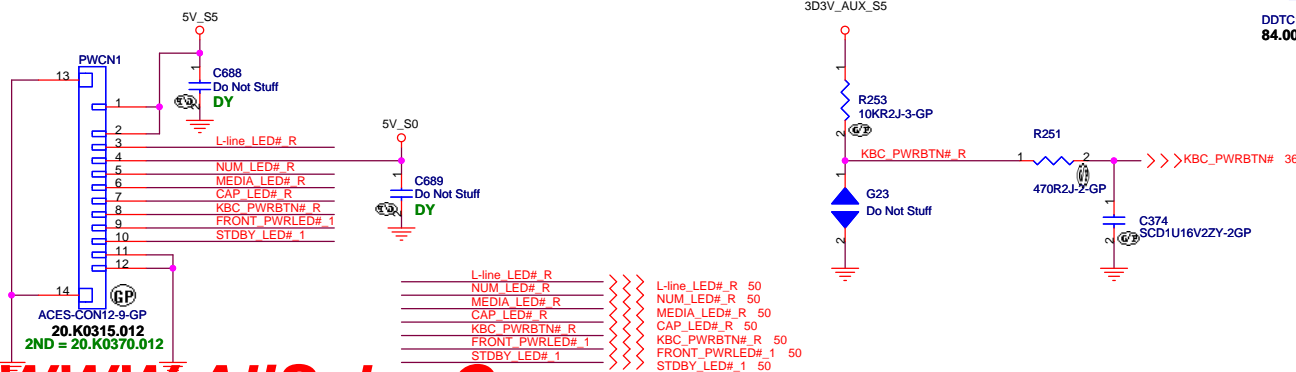
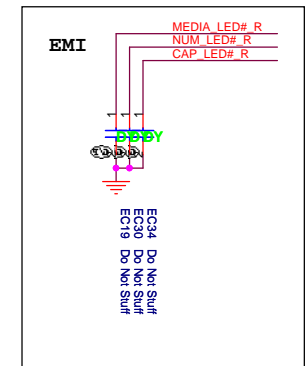
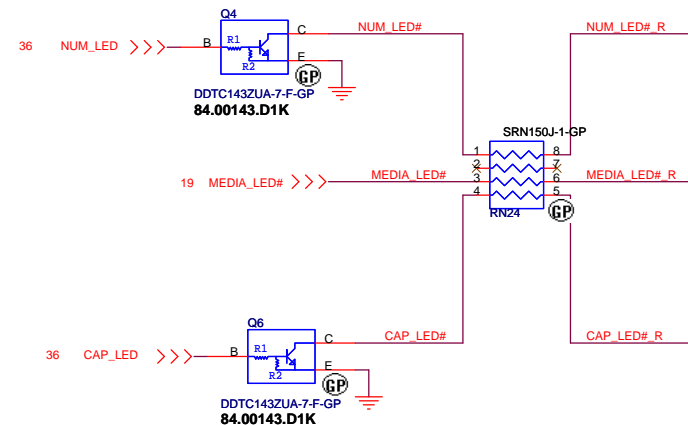
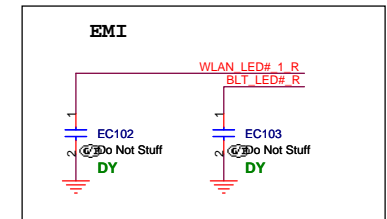
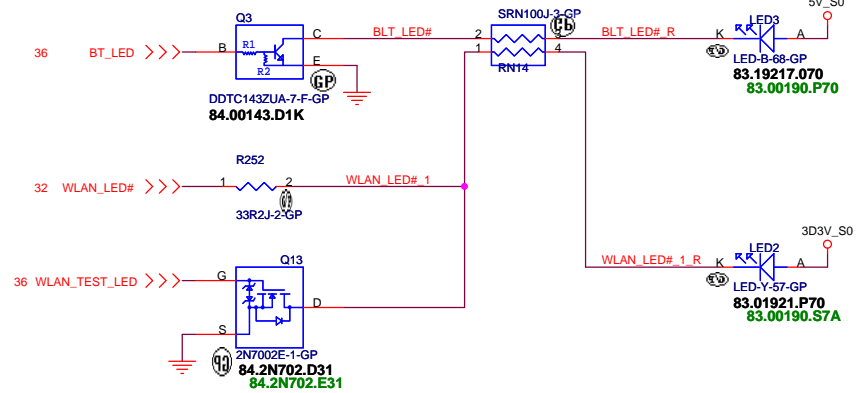
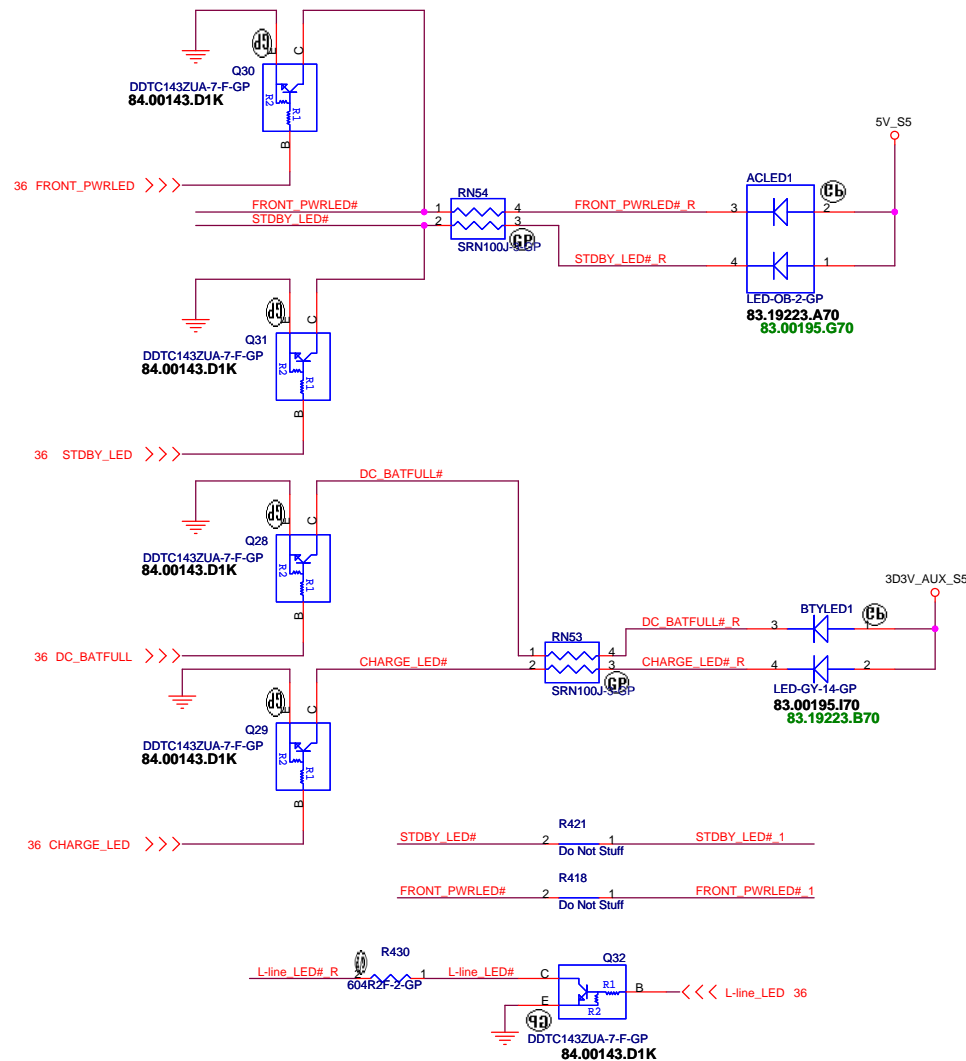


LCD/INVERTER/CCD CONN

Place close to MXM slot for BB2



Place close to MXM slot for BB2

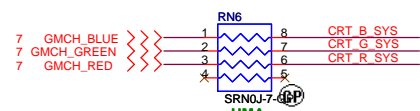
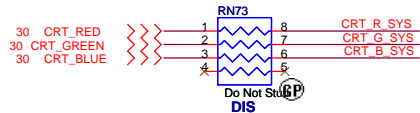
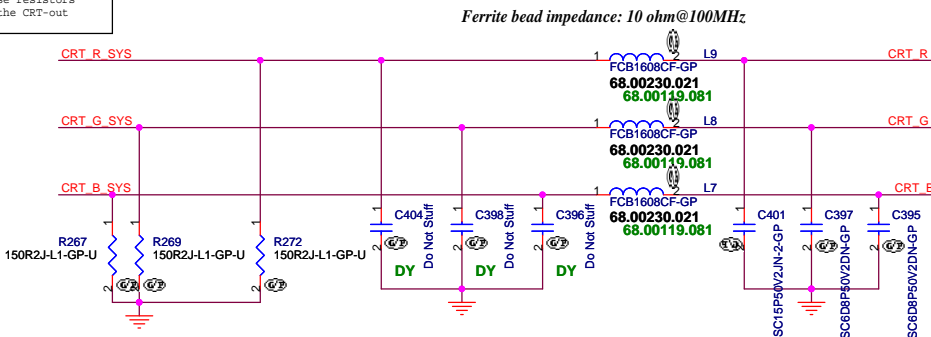


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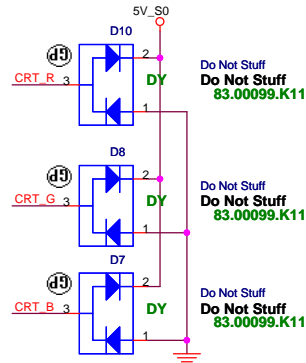
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Size	Document Number	Rev	
Date: Wednesday, October 22, 2008		Sheet 16	of 50
Big Bear 2		-1	

Layout Note:
Place these resistors
close to the CRT-out
connector

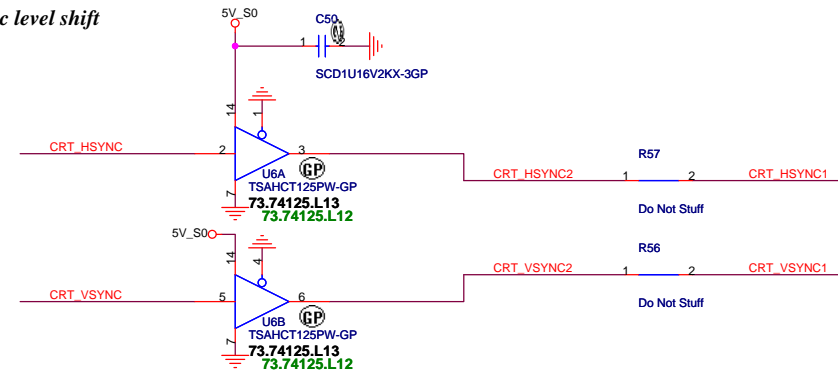


Layout Note:

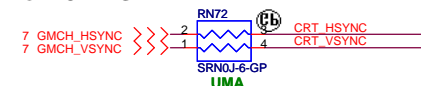
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



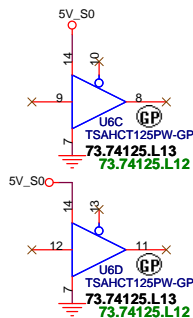
Hsync & Vsync level shift



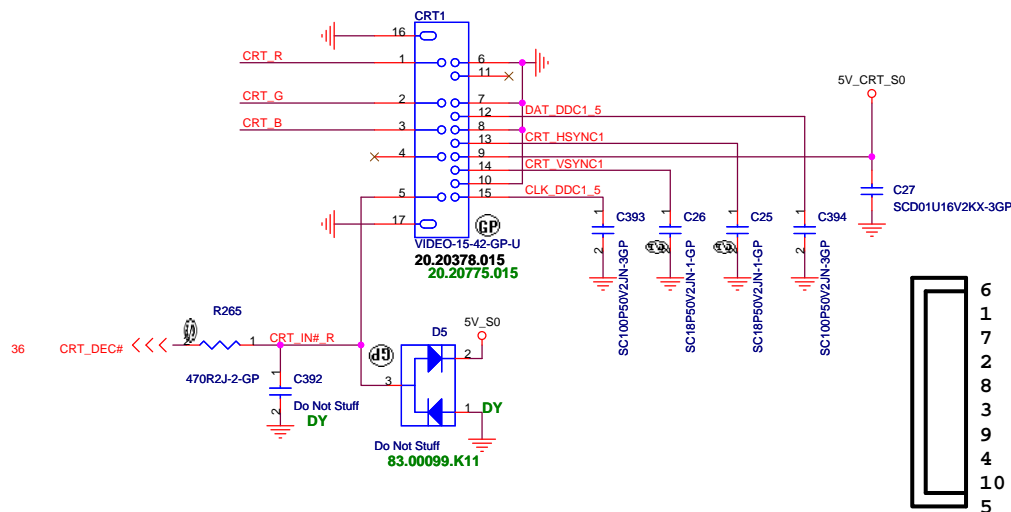
For UMA CRT



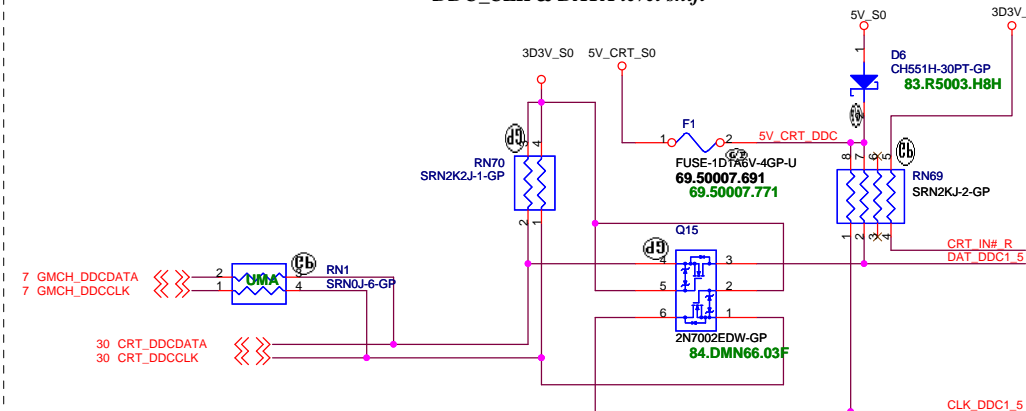
For DIS CRT



CRT I/F & CONNECTOR

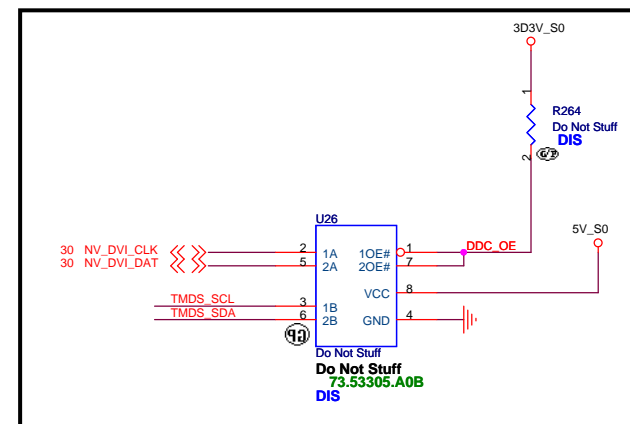


DDC_CLK & DATA level shift



UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.



Timing diagram for TMDS signals. The diagram shows four TMDS pairs (TMDS_A_TX0, TMDS_A_TX1, TMDS_A_TX2, TMDS_A_TX3) and their corresponding receiver signals (TMDS_TX0-, TMDS_TX0+, TMDS_TX1-, TMDS_TX1+, TMDS_TX2-, TMDS_TX2+, TMDS_TX3-, TMDS_TX3+). Each pair is connected to a receiver block (RN67, RN64, RN65, RN66) which outputs 'Do Not Stuff' and 'GP' signals. The receiver blocks are connected to a common bus. The diagram also shows a 'SKT-62' connector and a '62' pin number.

HDMI Interface Circuit Schematic

Components:

- R111: Do Not Stuff (DY)
- R47: Do Not Stuff (DY)
- R46: 4K7R2F-GP (UMA)
- R32: 499R2F-2-GP (UMA)
- R261: 1KR2J-1-GP (UMA)
- R39: 10KR2F-2-GP (UMA)
- R35: Do Not Stuff (DY)

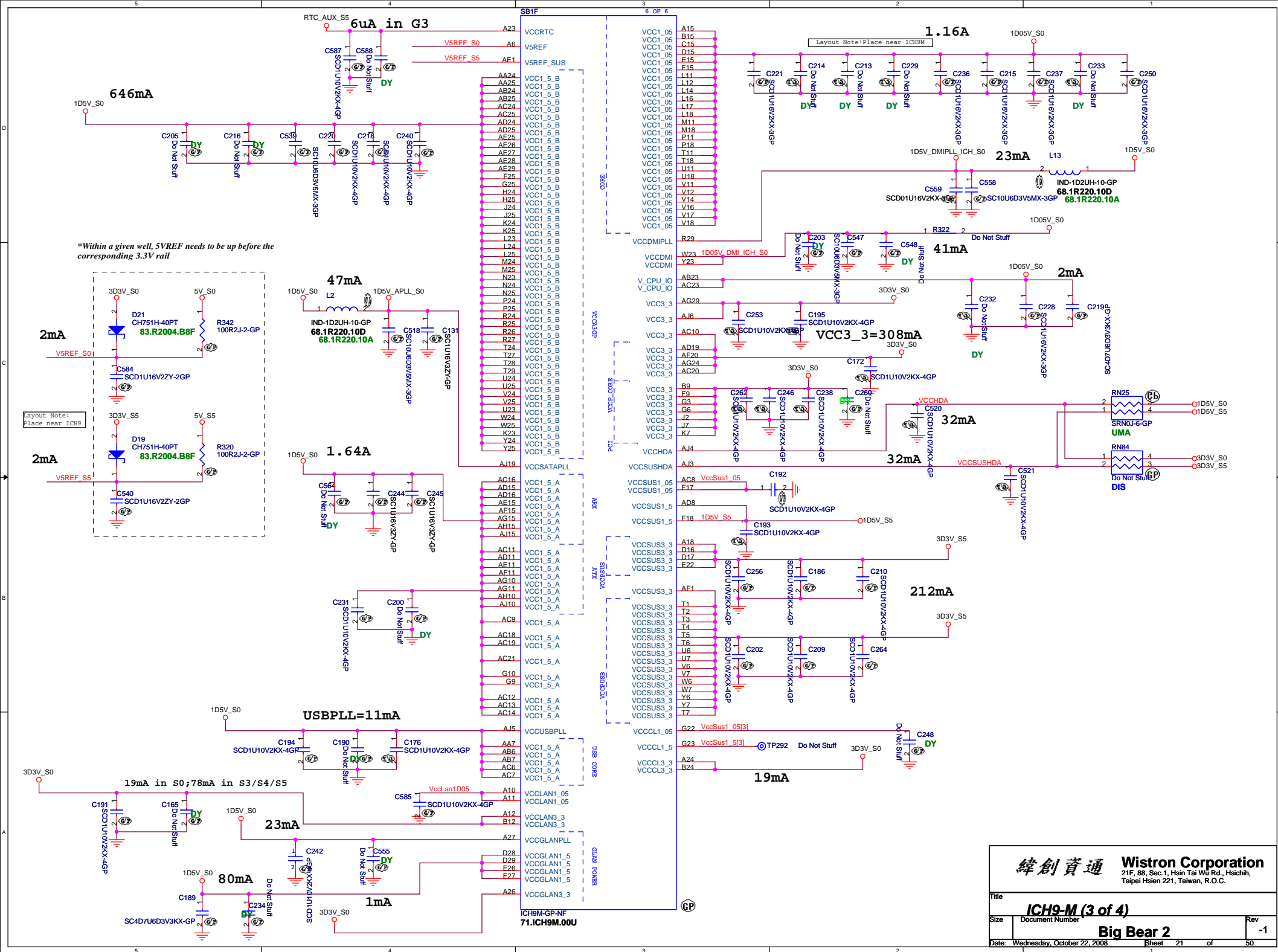
Power and Ground Connections:

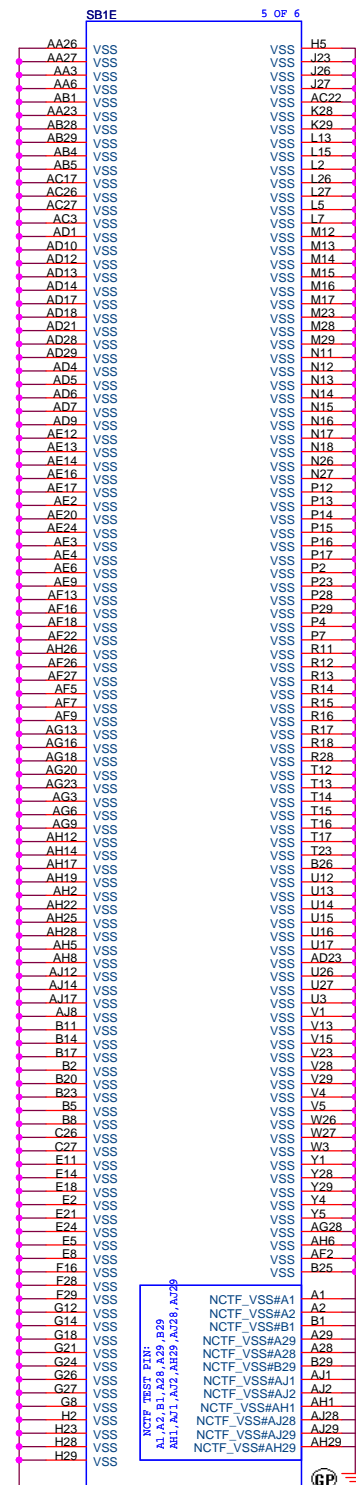
- 3D3V_S0
- 3D3V_S1
- GND

Signal Connections:

- HDMI_TX0+ MB
- HDMI_TX0- MB
- HDMI_TXC+ MB
- HDMI_TXC- MB
- HDMI_CLK+ MB
- HDMI_CLK- MB
- HDMI_DATA0+ MB
- HDMI_DATA0- MB
- HDMI_DATA1+ MB
- HDMI_DATA1- MB
- HDMI_DATA2+ MB
- HDMI_DATA2- MB
- HDMI_DATA3+ MB
- HDMI_DATA3- MB
- HDMI_DATA4+ MB
- HDMI_DATA4- MB
- HDMI_DATA5+ MB
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- HDMI_DATA148- MB
- HDMI





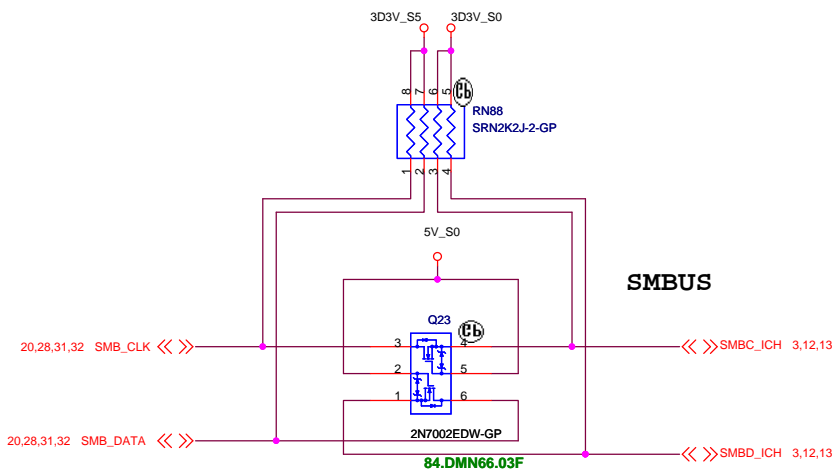


NCTF TEST PIN:
A1, A2, B1, A28, A29, B29,
AH1, AH2, AH28, AH29, AJ28,
AJ29

ICH9M-GP-NF
71.1C 100U



- TP195 Do Not Stuff
- TP194 Do Not Stuff
- TP190 Do Not Stuff
- TP193 Do Not Stuff
- TP187 Do Not Stuff
- TP191 Do Not Stuff
- TP313 Do Not Stuff
- TP314 Do Not Stuff
- TP174 Do Not Stuff
- TP315 Do Not Stuff
- TP172 Do Not Stuff
- TP175 Do Not Stuff



緯創資通

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Title

ICH9-M (4 of 4)

Size

Document Number

Rev

-1

Date

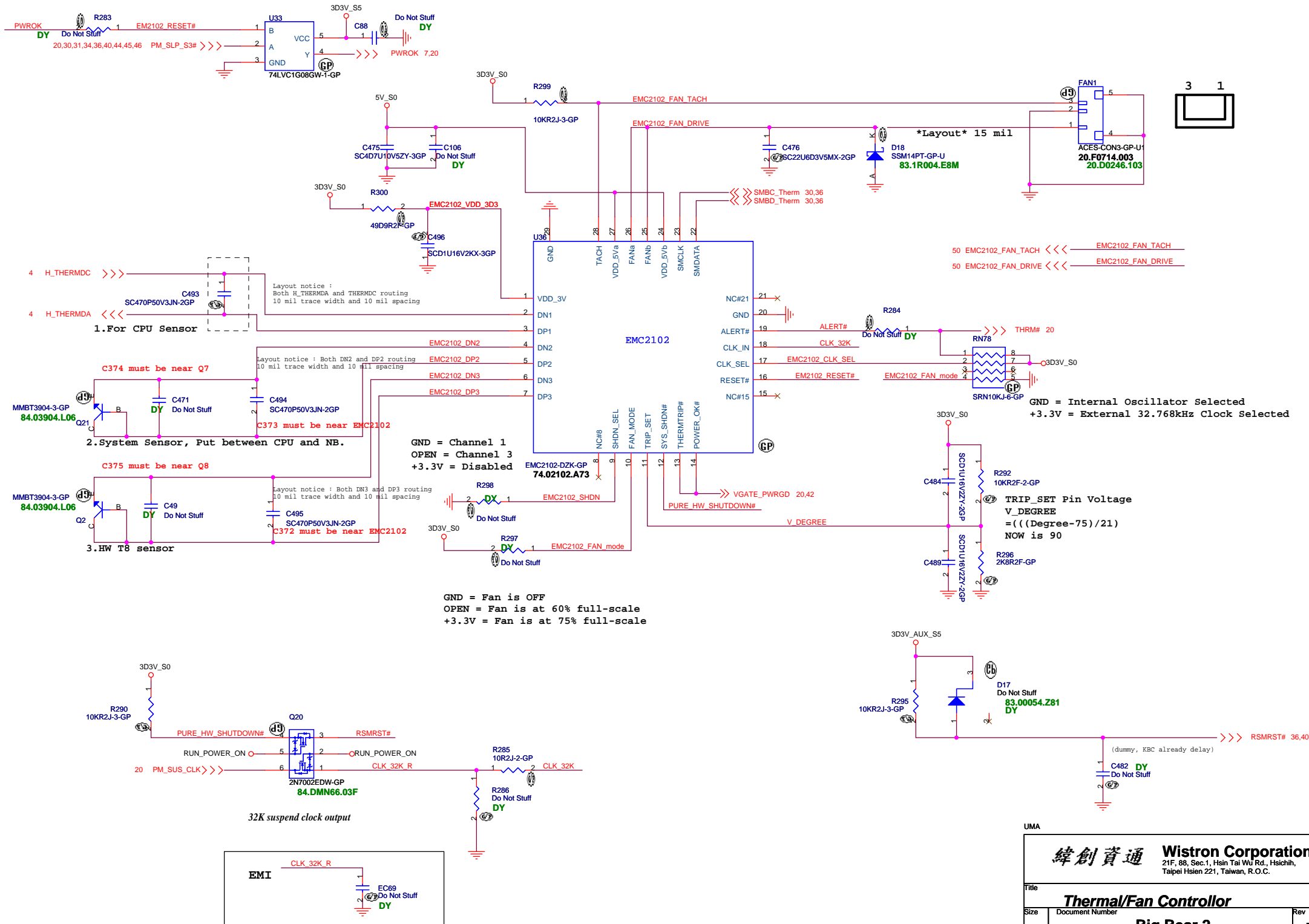
Wednesday, October 22, 2008

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22

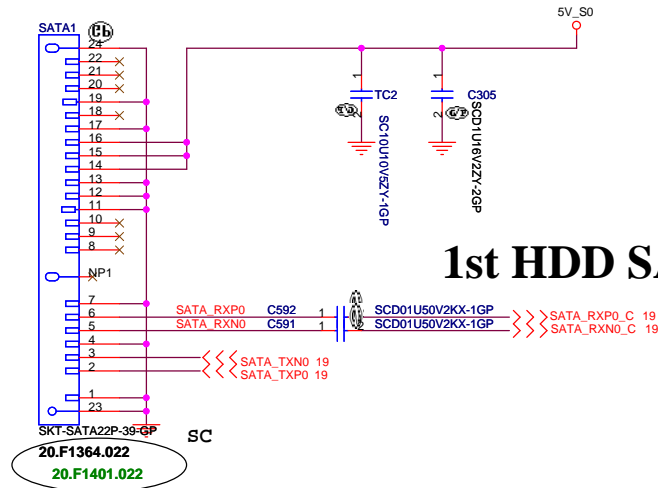
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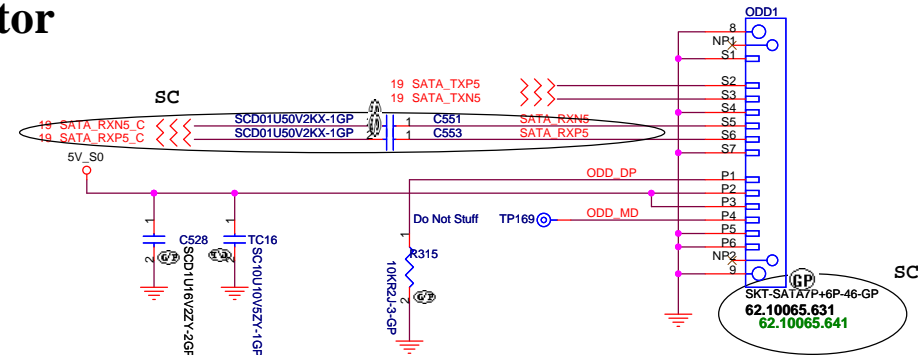
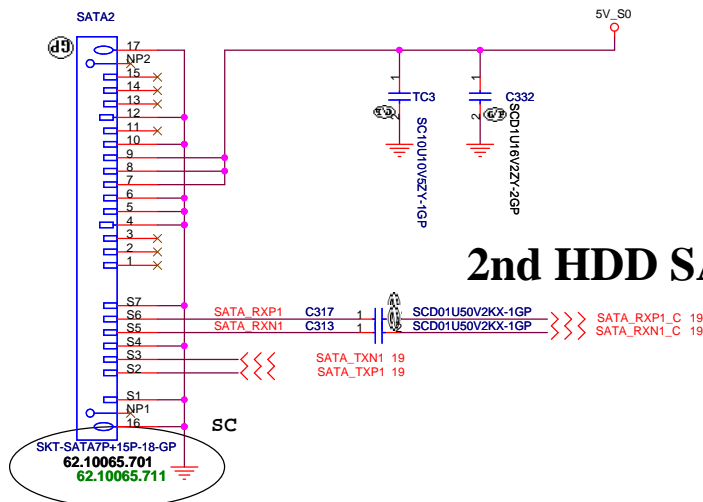


SATA ODD Connector

1st HDD SATA Connector

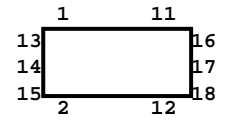
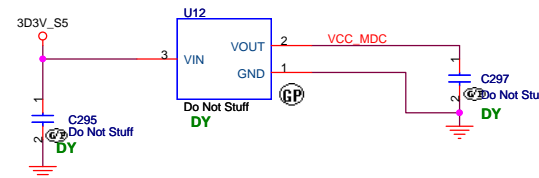
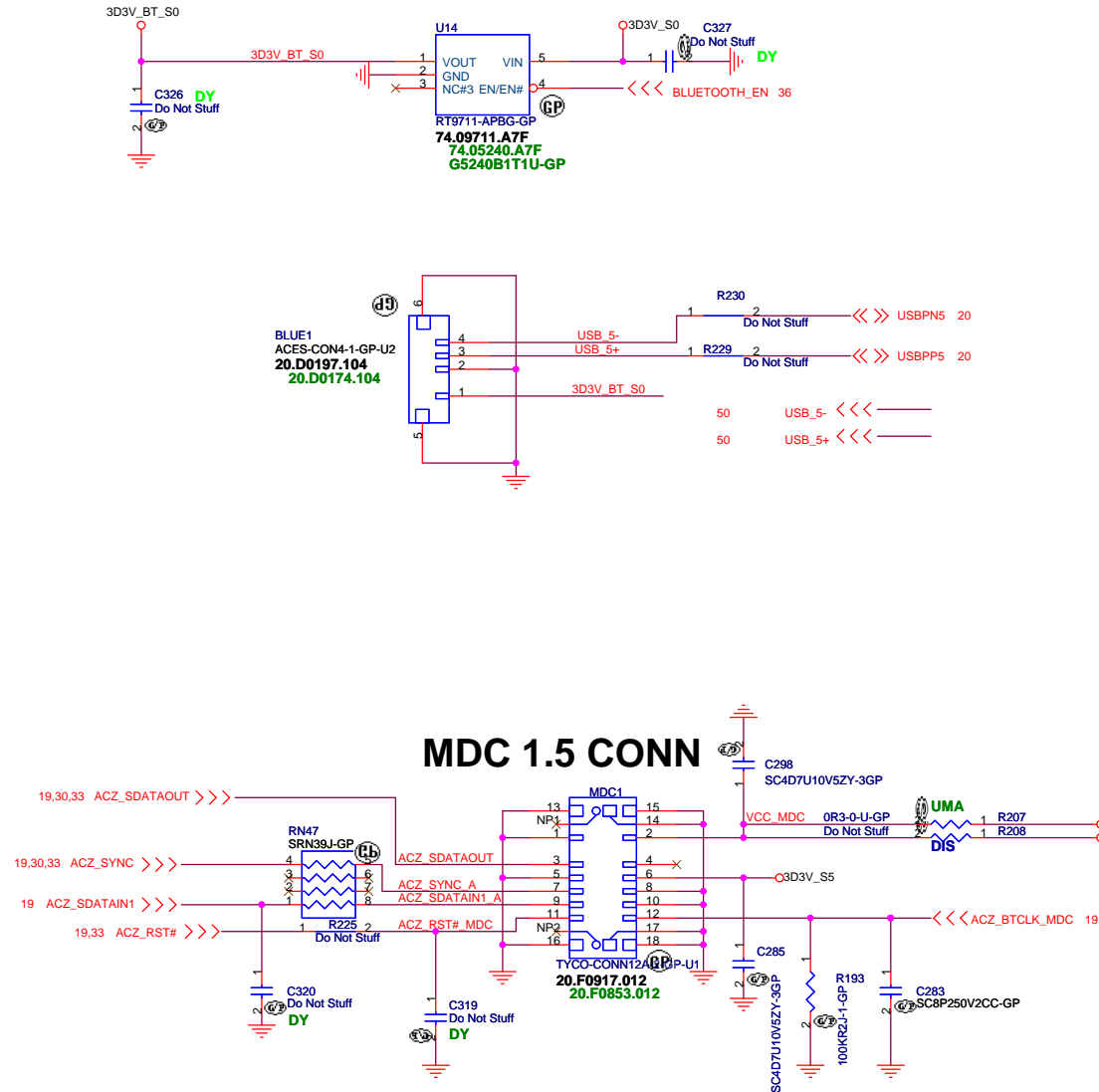


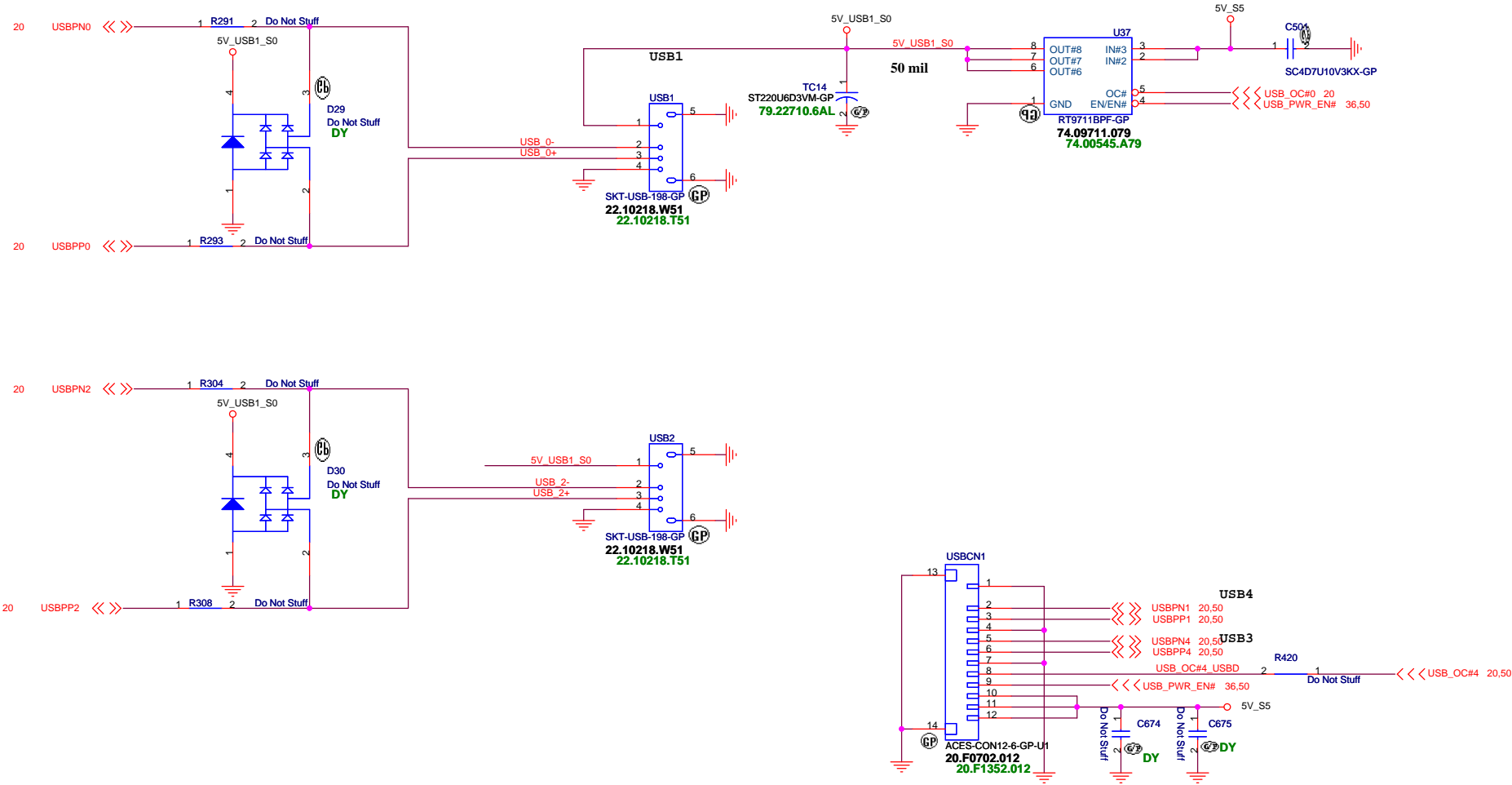
2nd HDD SATA Connector

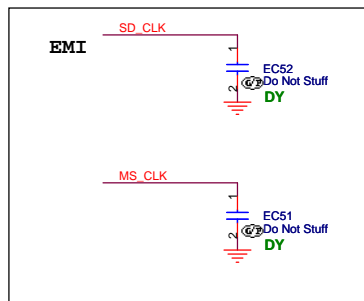
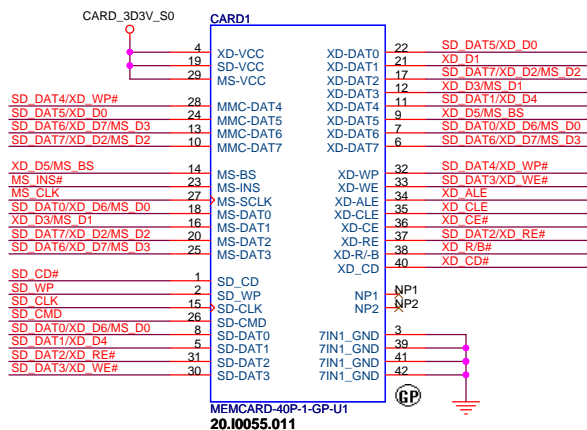


BLUETOOTH MODULE

1.5A / High Active Voltage 2V







Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Realtek Card Reader

Size	Document Number
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Big Bear 2

-1

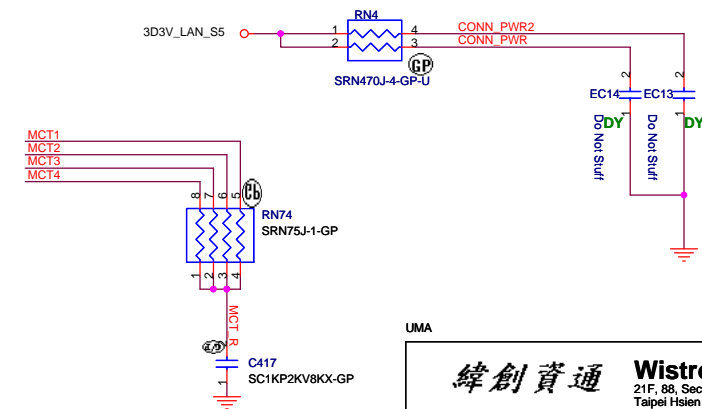
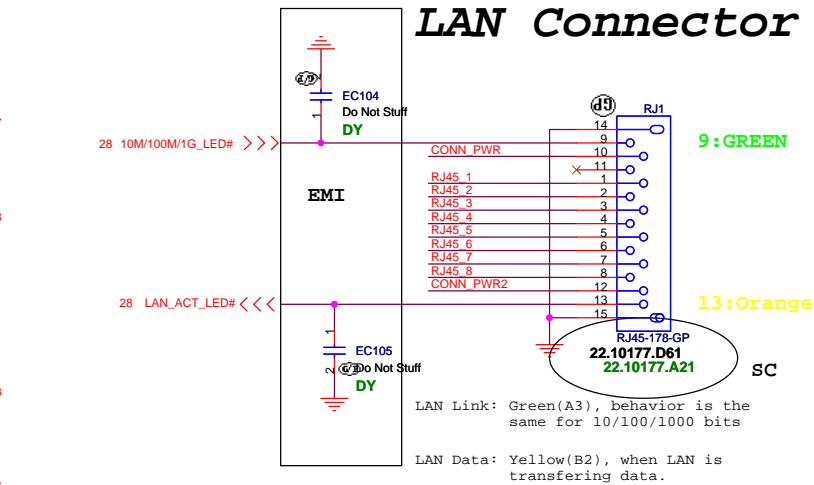
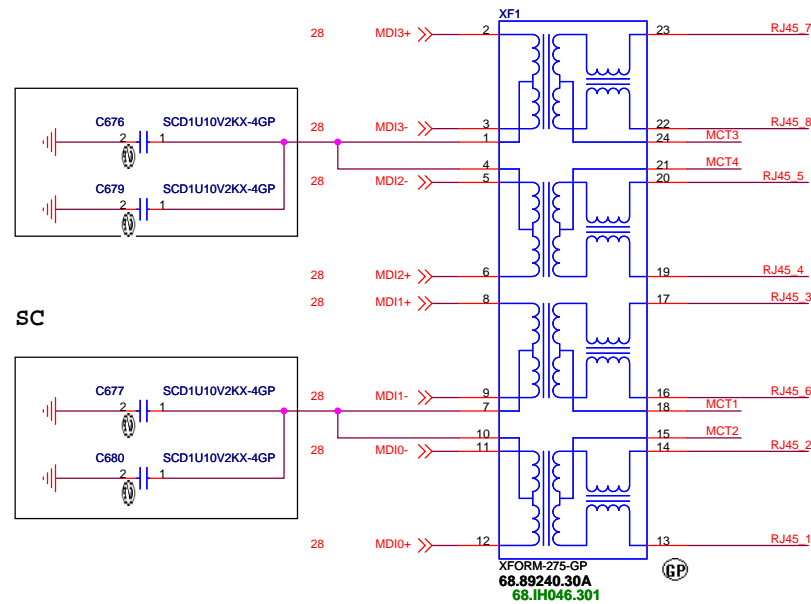
Date: Wednesday, October 22, 2008

Sheet 27 of



LAN Connector

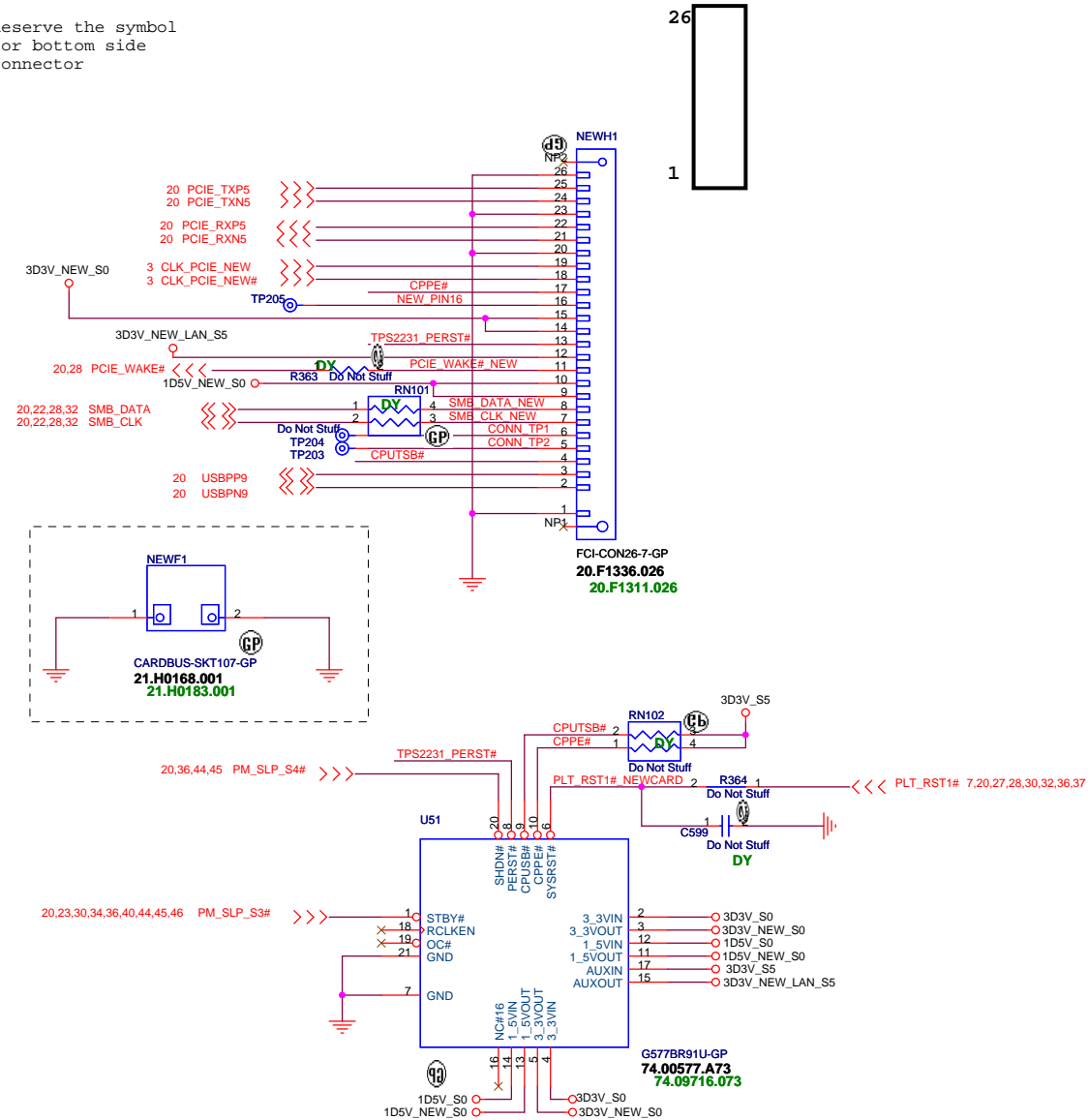
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



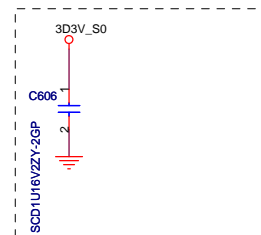
NEWCARD Connector

Reserve the symbol
for bottom side
connector

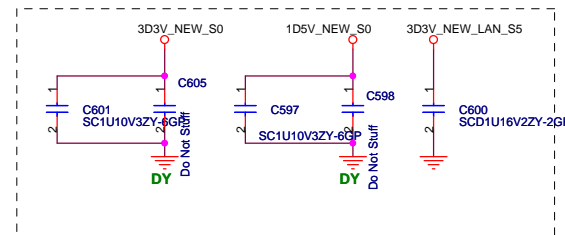
TOP VIEW



Place them Near to Chip



Place them Near to Connector

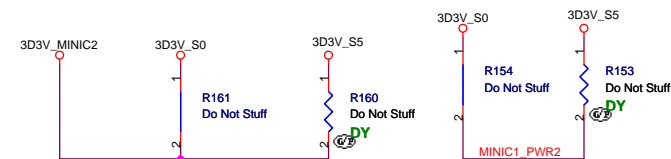
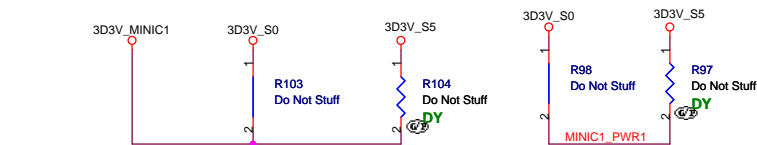


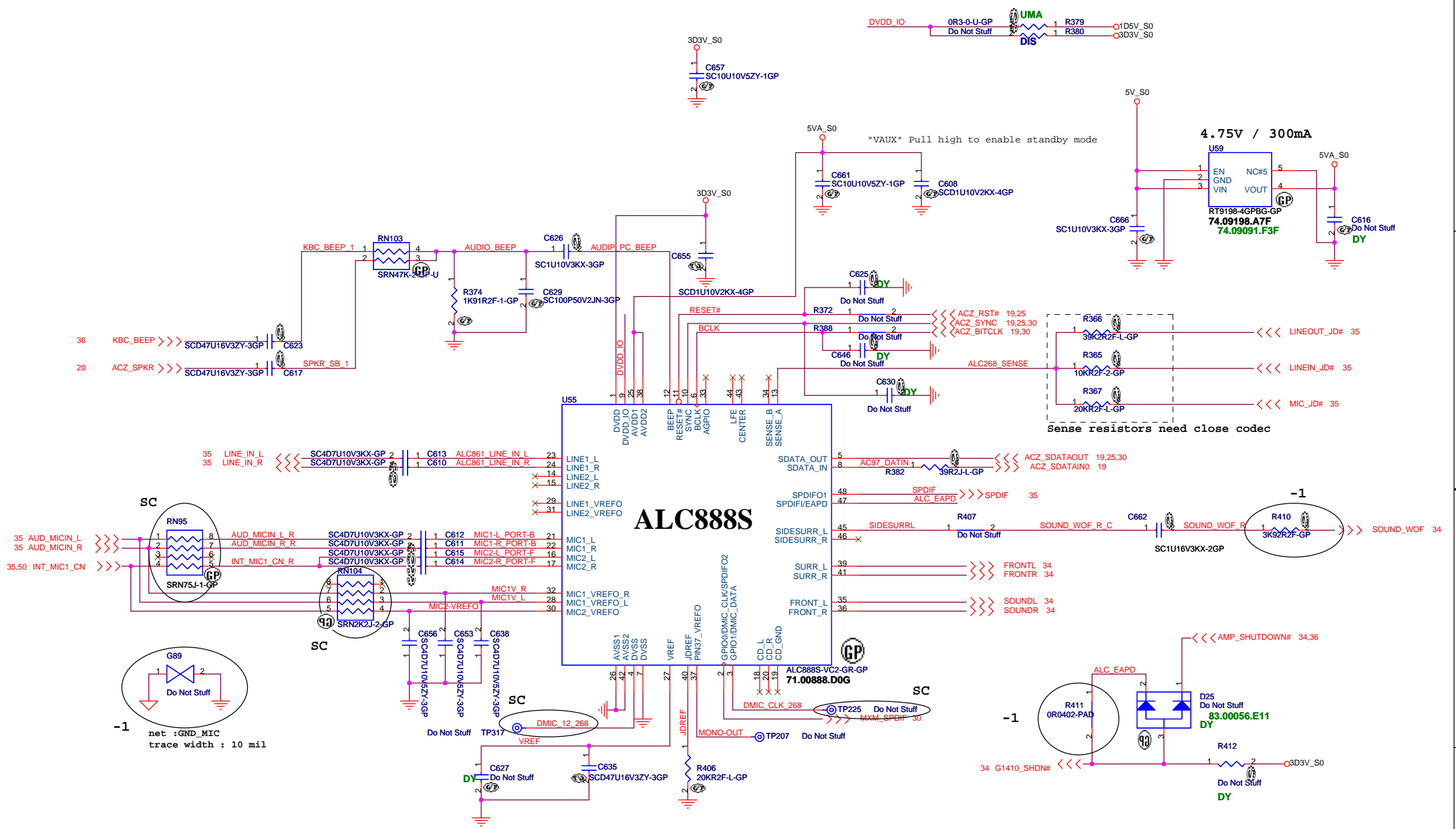
UMA

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Taipei Hsien 221, Taiwan, R.O.C.

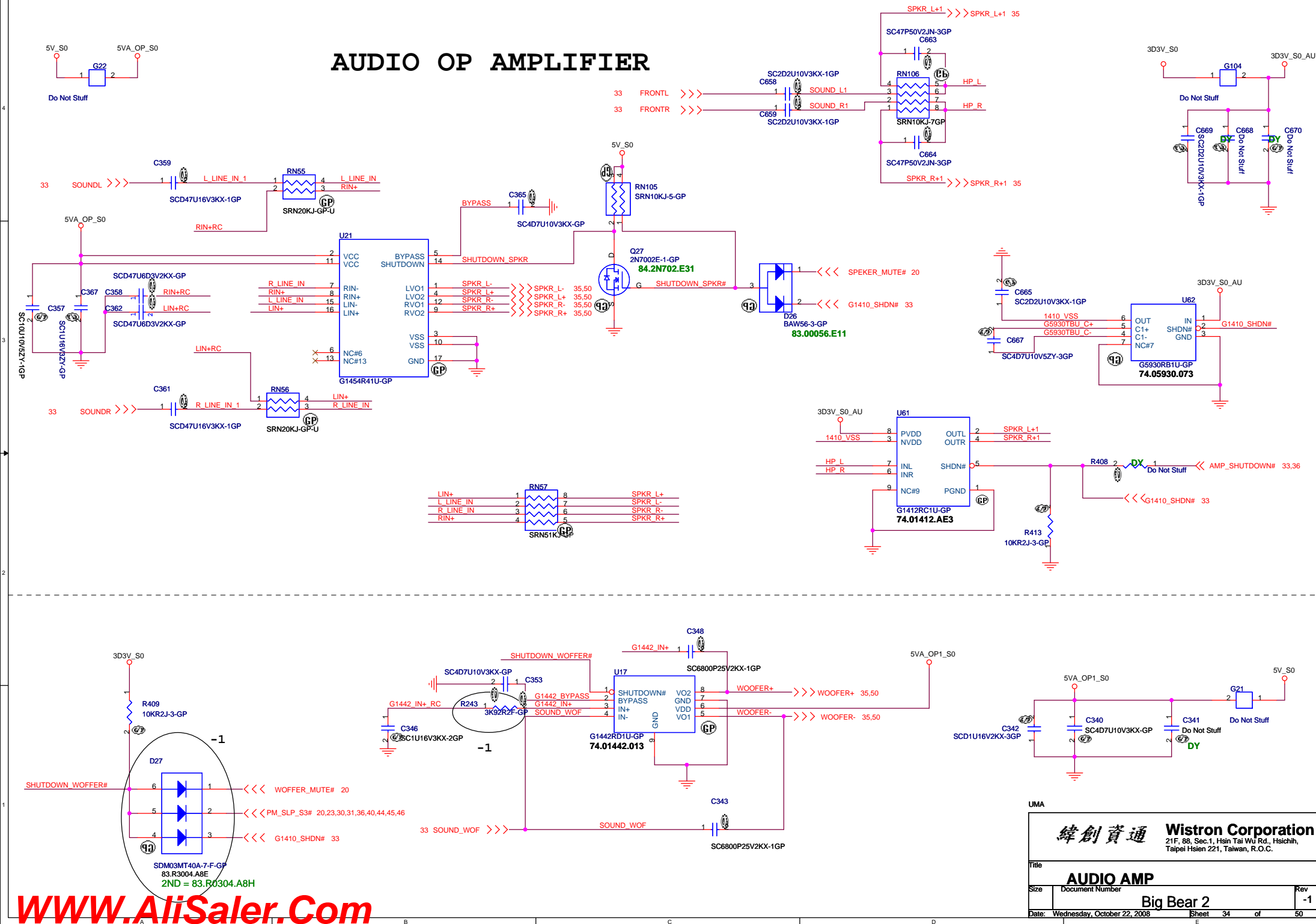
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Size	Document Number	Rev
Big Bear 2		-1
Date: Wednesday, October 22, 2008	Sheet 31 of 50	

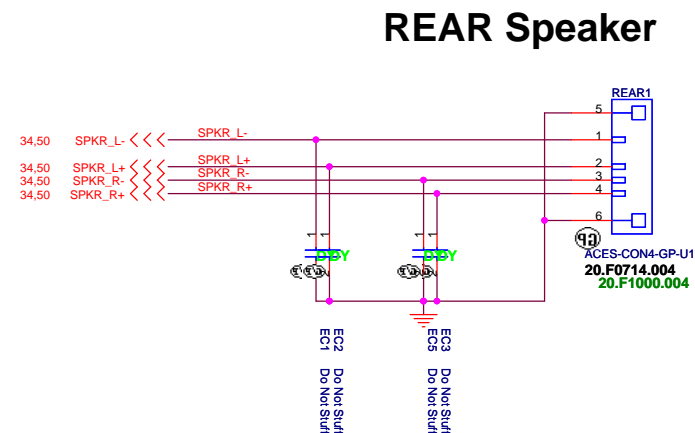
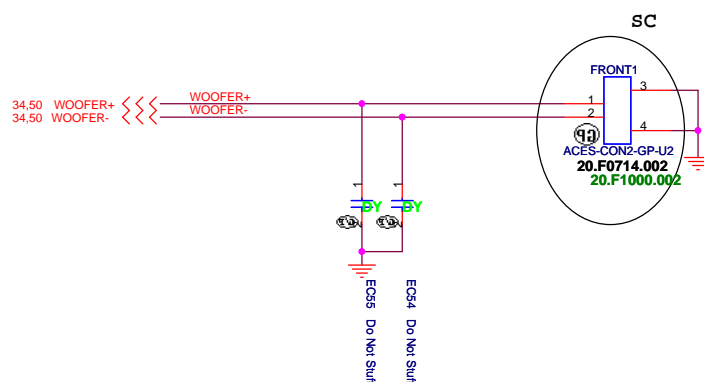
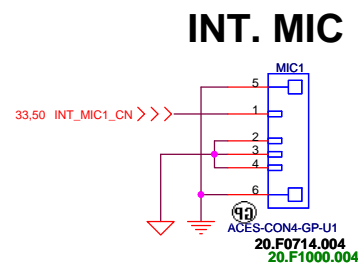
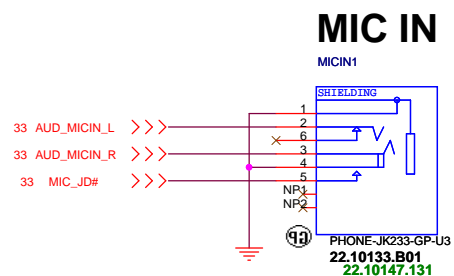
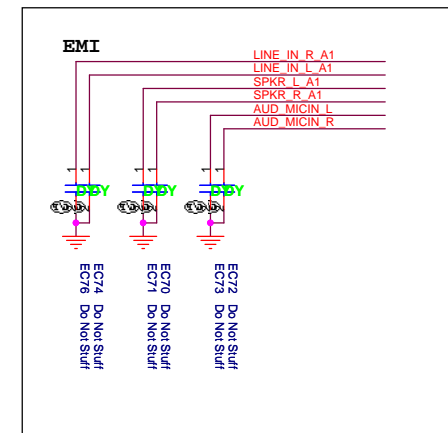
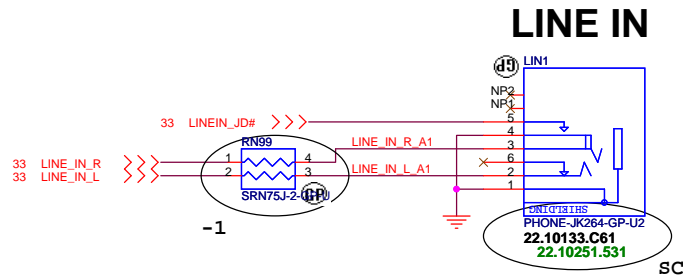
WWW.AliSaler.Com

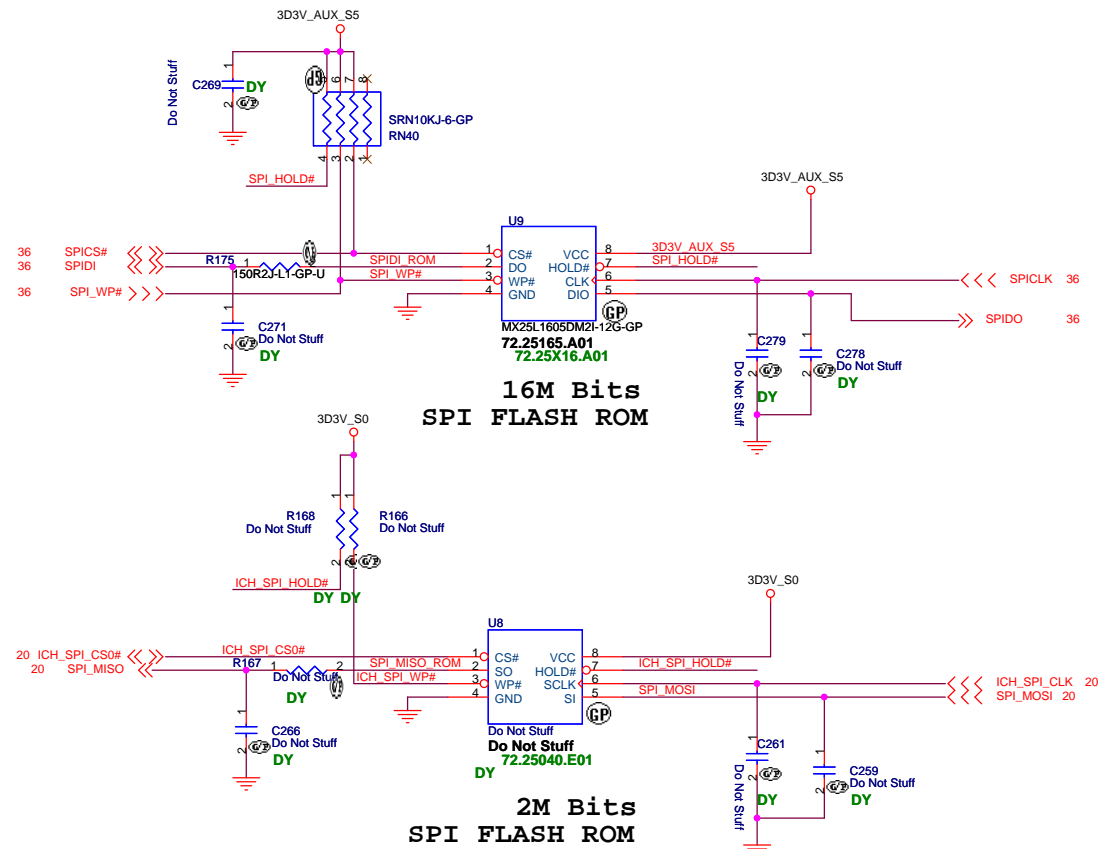




AUDIO OP AMPLIFIER







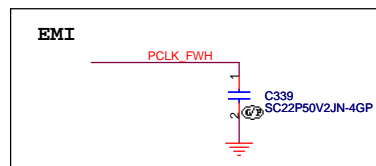
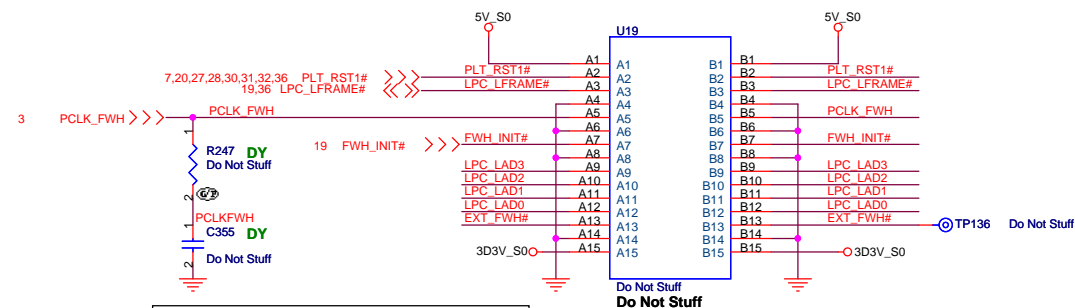
TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

19,36 LPC_LAD[0..3] <<< LPC_LAD[0..3]

GOLDEN FINGER FOR DEBUG BOARD

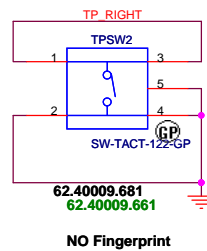
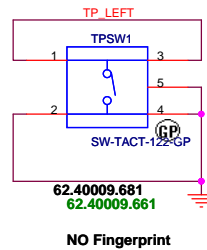
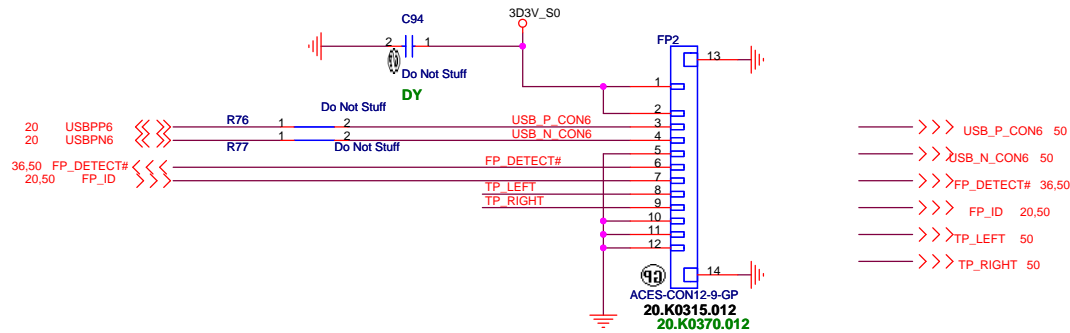


UMA

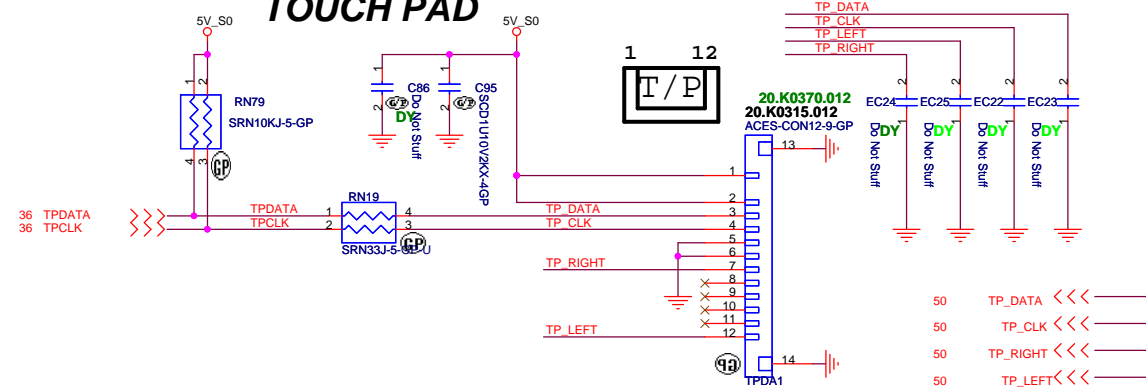
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
BIOS		
Size	Document Number	Rev
	Big Bear 2	-1
Date:	Wednesday, October 22, 2008	Sheet 37 of 50

Finger printer



TOUCH PAD

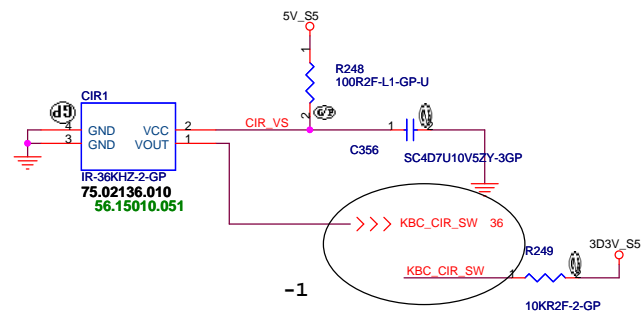


UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Finger Printer and Touch PAD			
Size A3	Document Number		Rev
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Date:	Wednesday, October 22, 2008	Sheet 38 of 50	

CIR Module

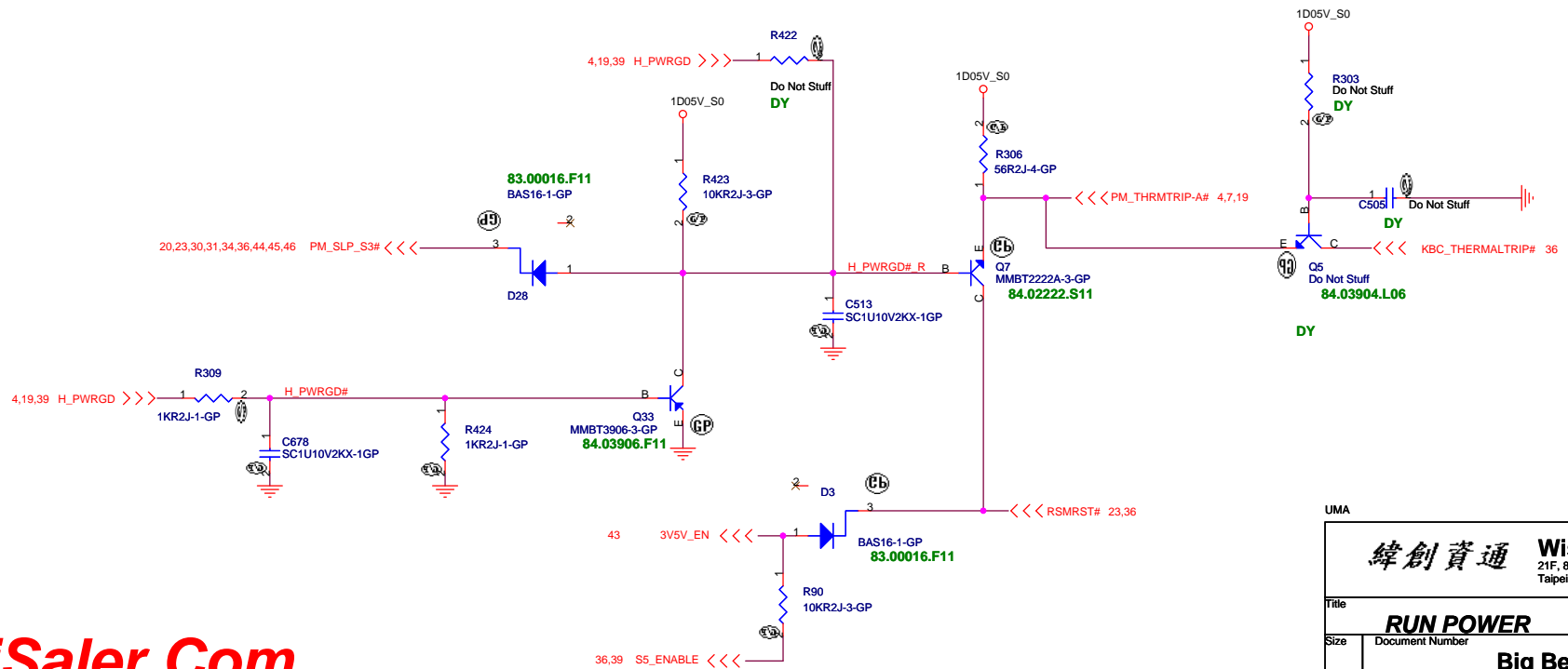
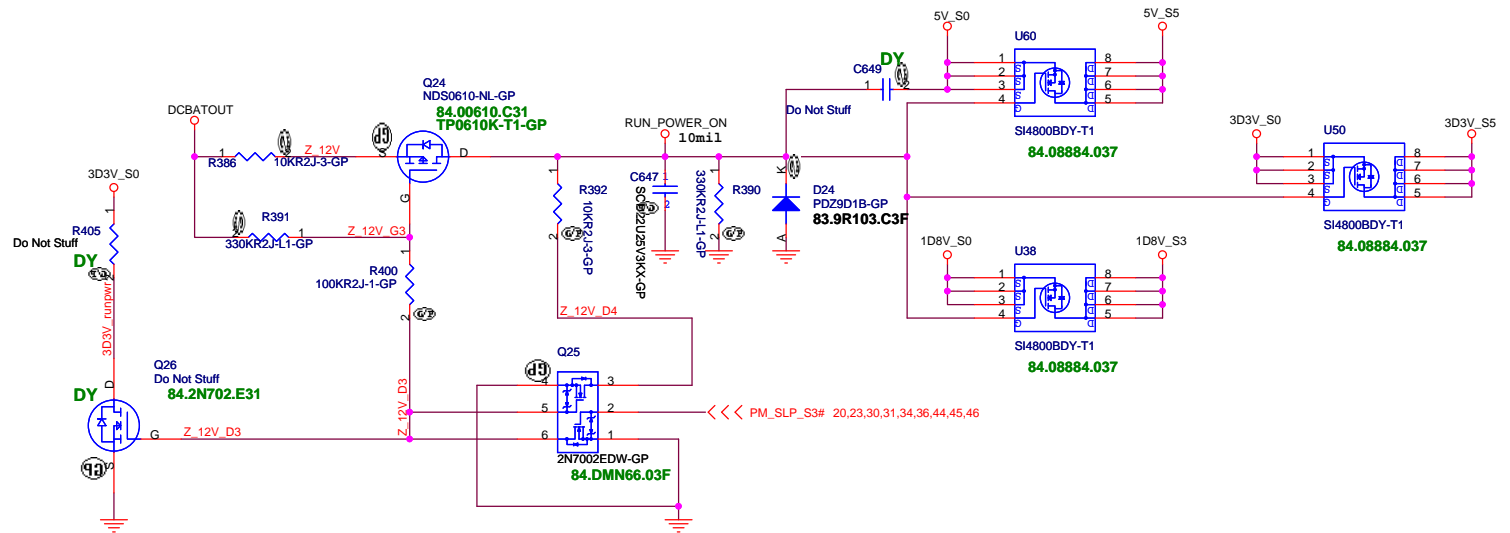


Check test point

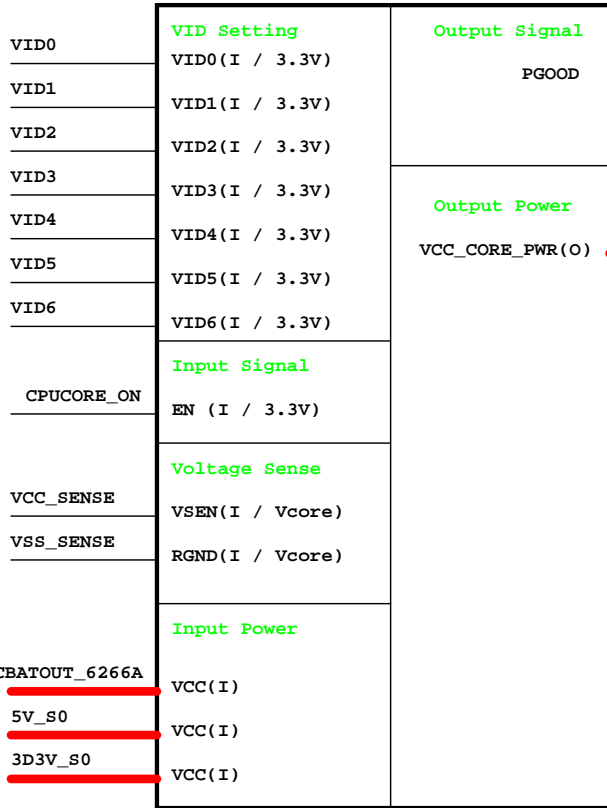
- 3D3V_S0 ○ ———— ● TP202 Do Not Stuff
- 3D3V_AUX_S5 ○ ———— ● TP141 Do Not Stuff
- 3D3V_S5 ○ ———— ● TP120 Do Not Stuff
- 5V_S5 ○ ———— ● TP130 Do Not Stuff
- 20,36 PM_PWRBTN# <<< ———— ● TP115 Do Not Stuff
- 4,19,40 H_PWRGD <<< ———— ● TP320 Do Not Stuff
- 36,40 S5_ENABLE <<< ———— ● TP110 Do Not Stuff
- 4,6 H_CPURST# <<< ———— ● TP278 Do Not Stuff

Test Point 放在 Dimm Door 打開可量測處

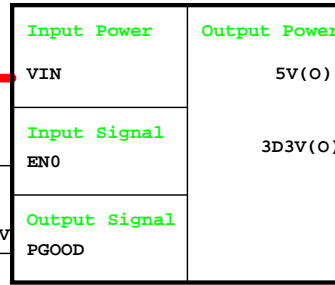
Run Power



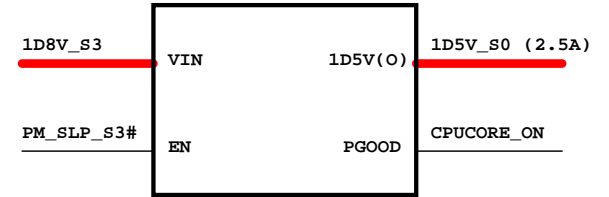
CPU_CORE
ISL6266A



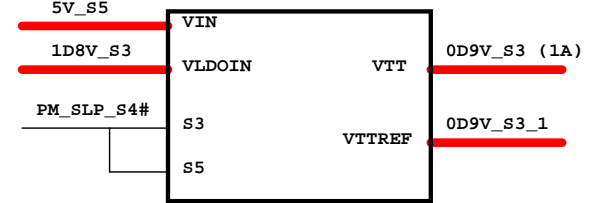
TPS51125
5V/3D3V



RT9018A
1D5V_S0



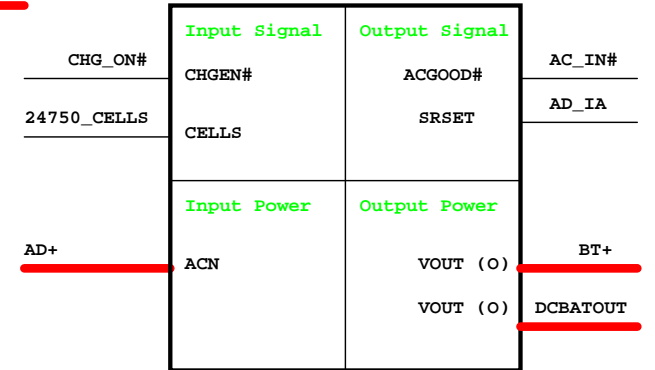
RT9026 0D9V_S0



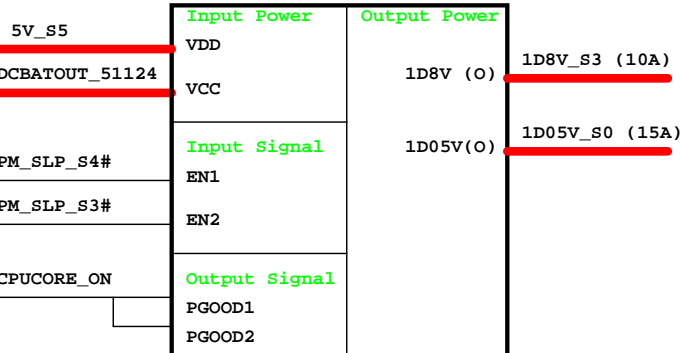
G9131 2D5V_S0



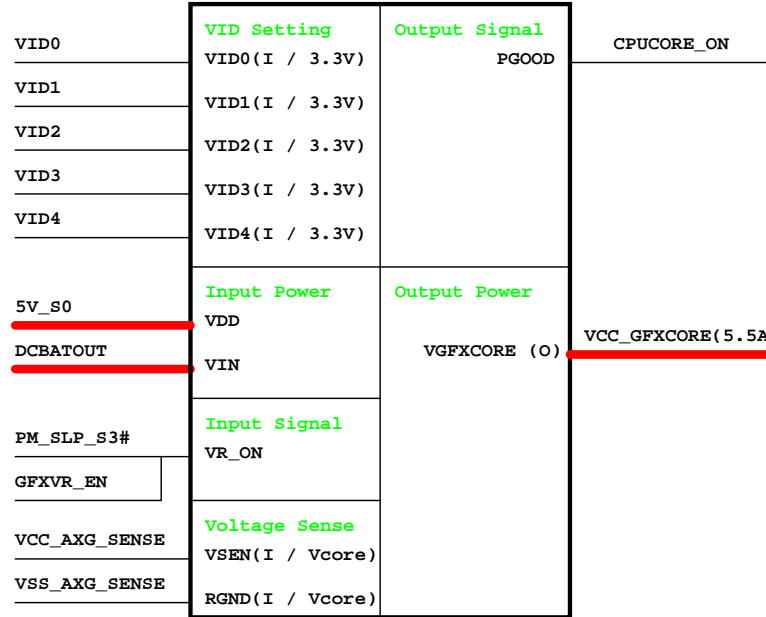
Charger BQ24750



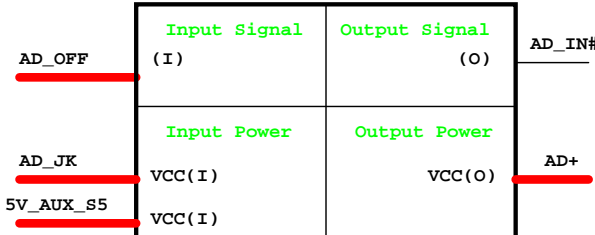
TPS51124
1D8V/1D05V



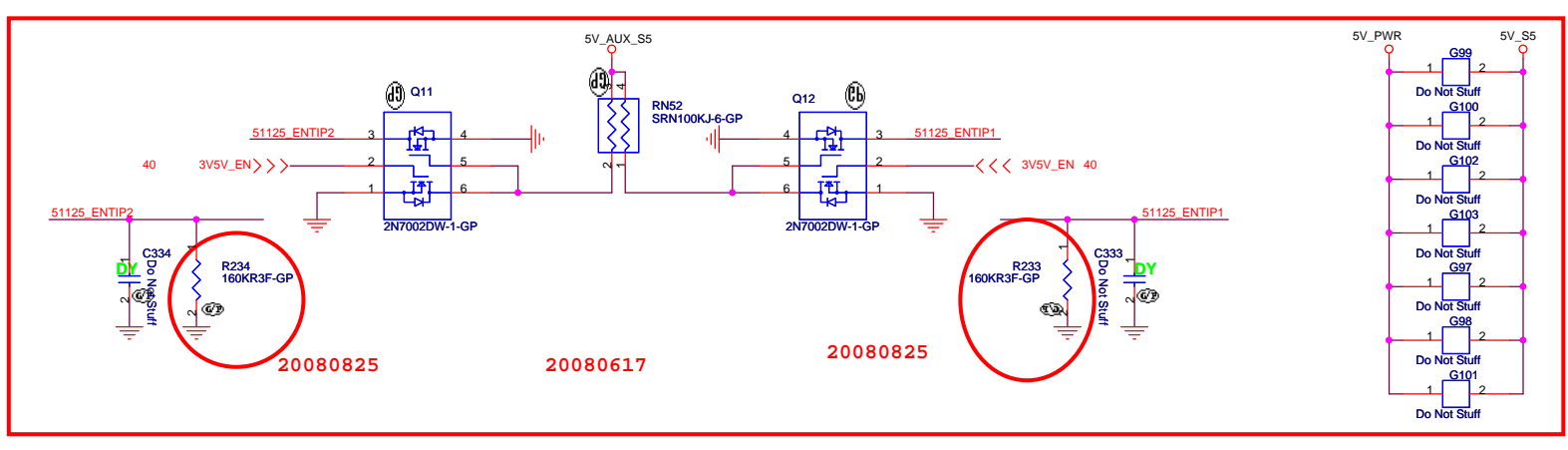
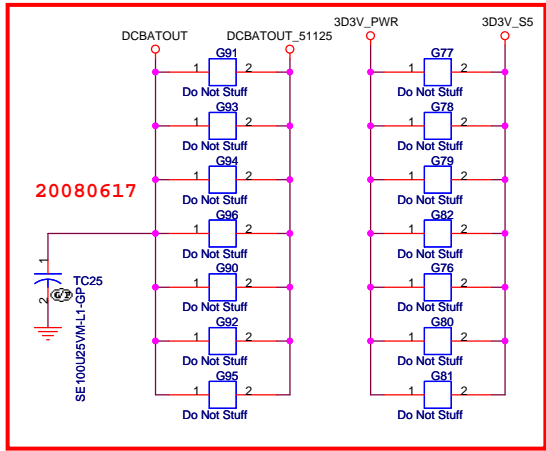
GFX_CORE
ISL6263A



Adapter

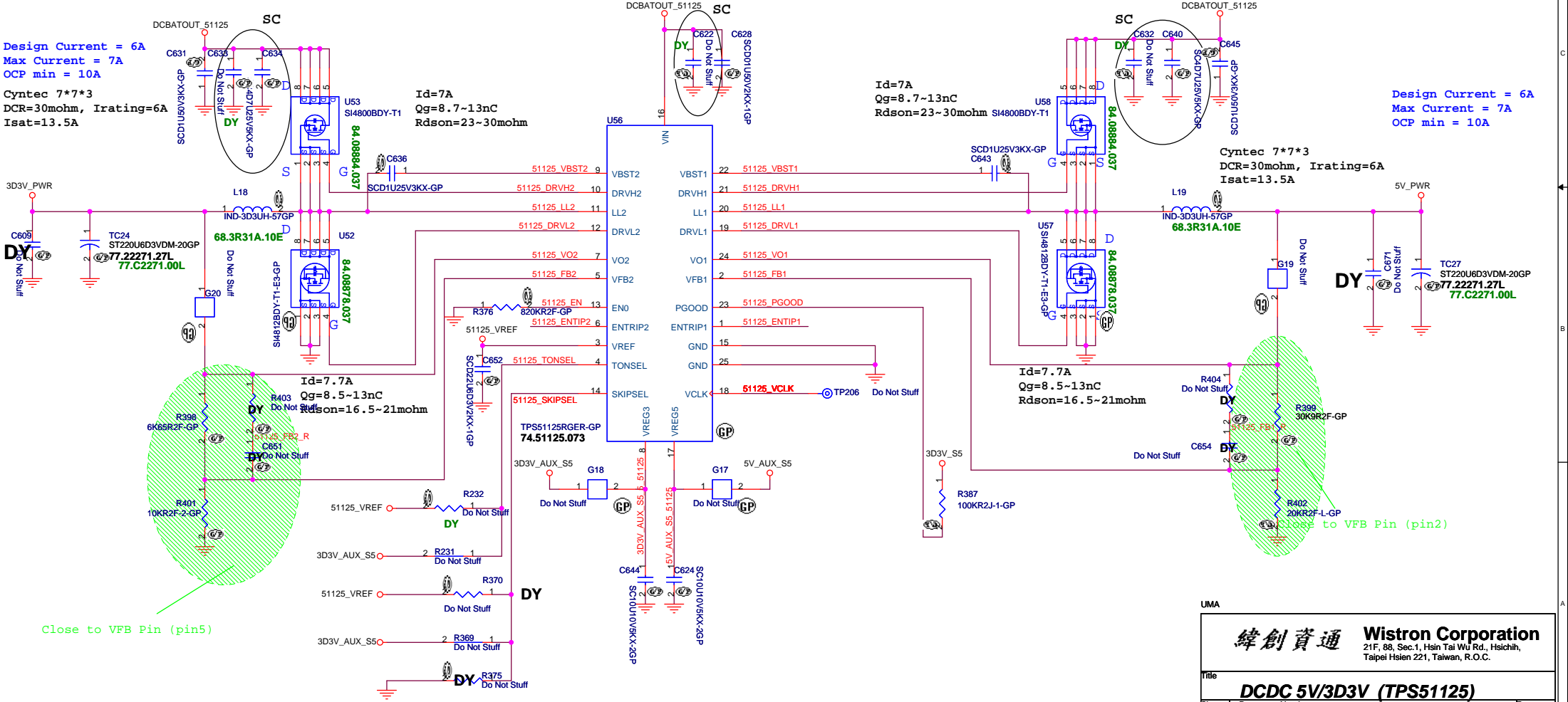


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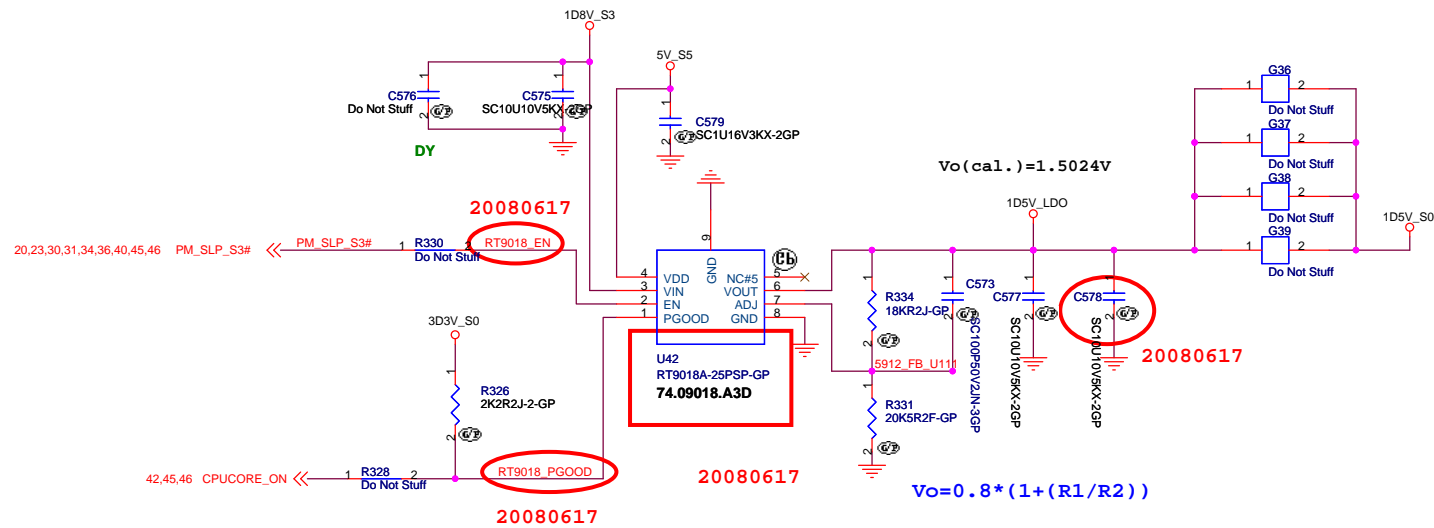
Design Current = 6A
Max Current = 7A
OCP min = 10A

Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A

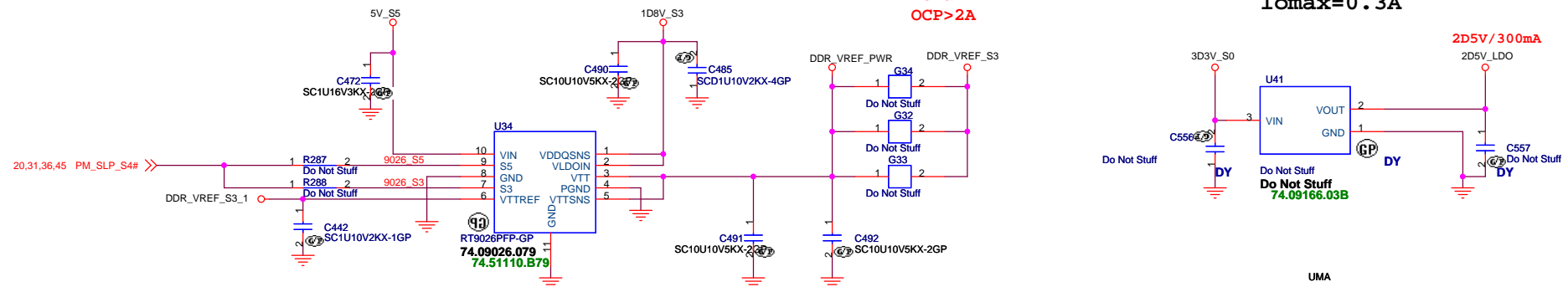


Close to VFB Pin (pin5)

1D5V_S0
Iomax=2.5A



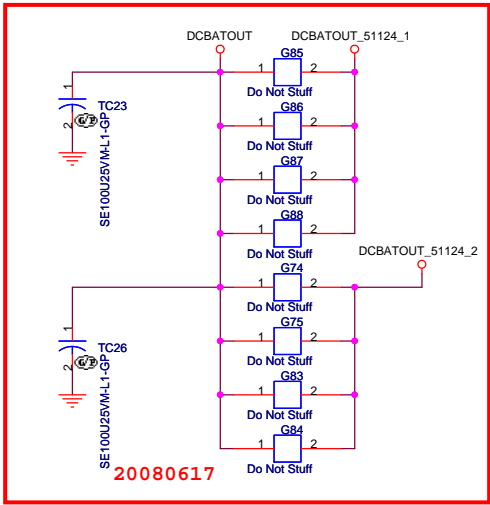
2D5V_S0
Iomax=0.3A



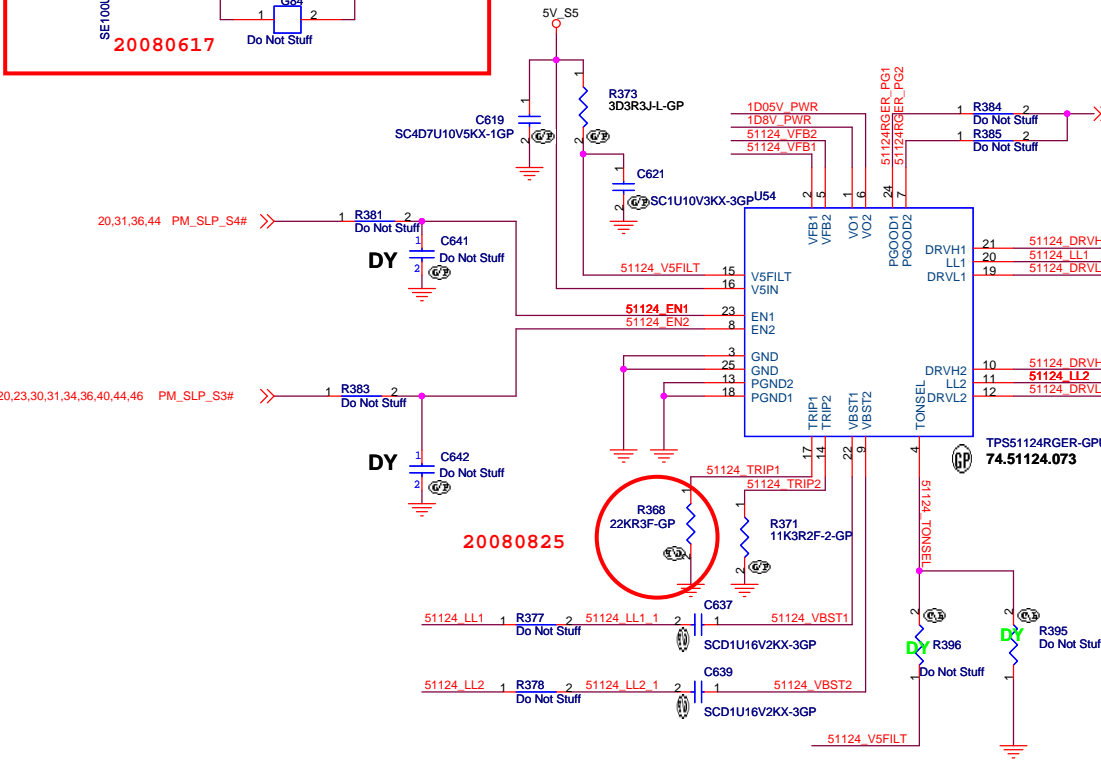
UMA

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Title			
1D5V & 0D9V & 2D5V			
Size A3	Document Number		Rev
	Big Bear 2		-1
Date:	Wednesday, October 22, 2008	Sheet 44 of	50

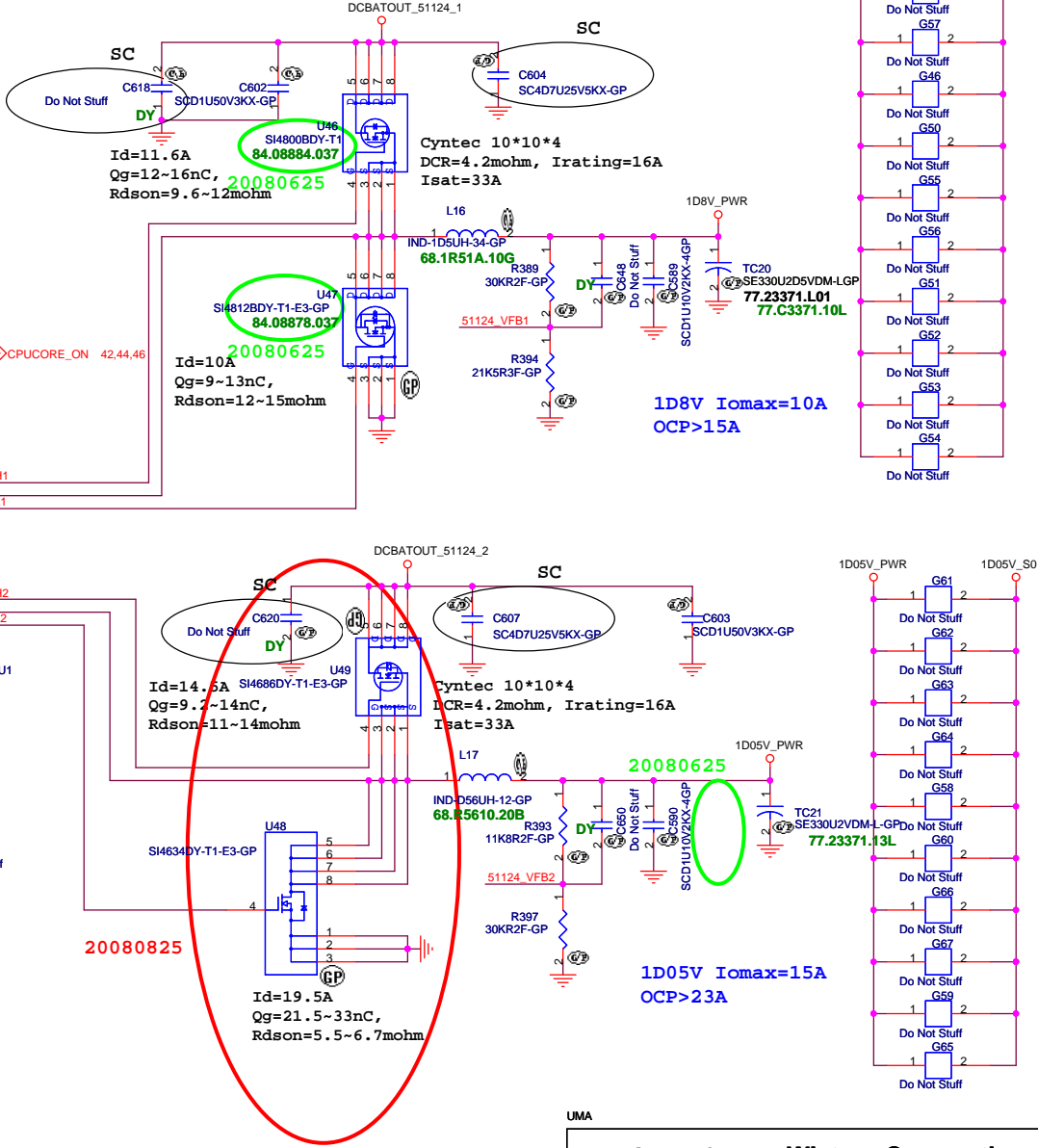


$V_{trip}(mV) = R_{trip}(Kohm) * I_0(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$
 I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

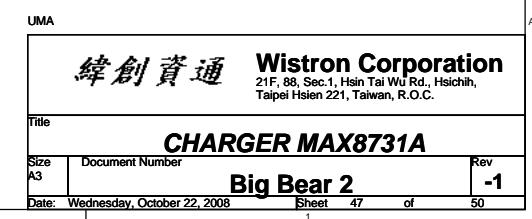


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

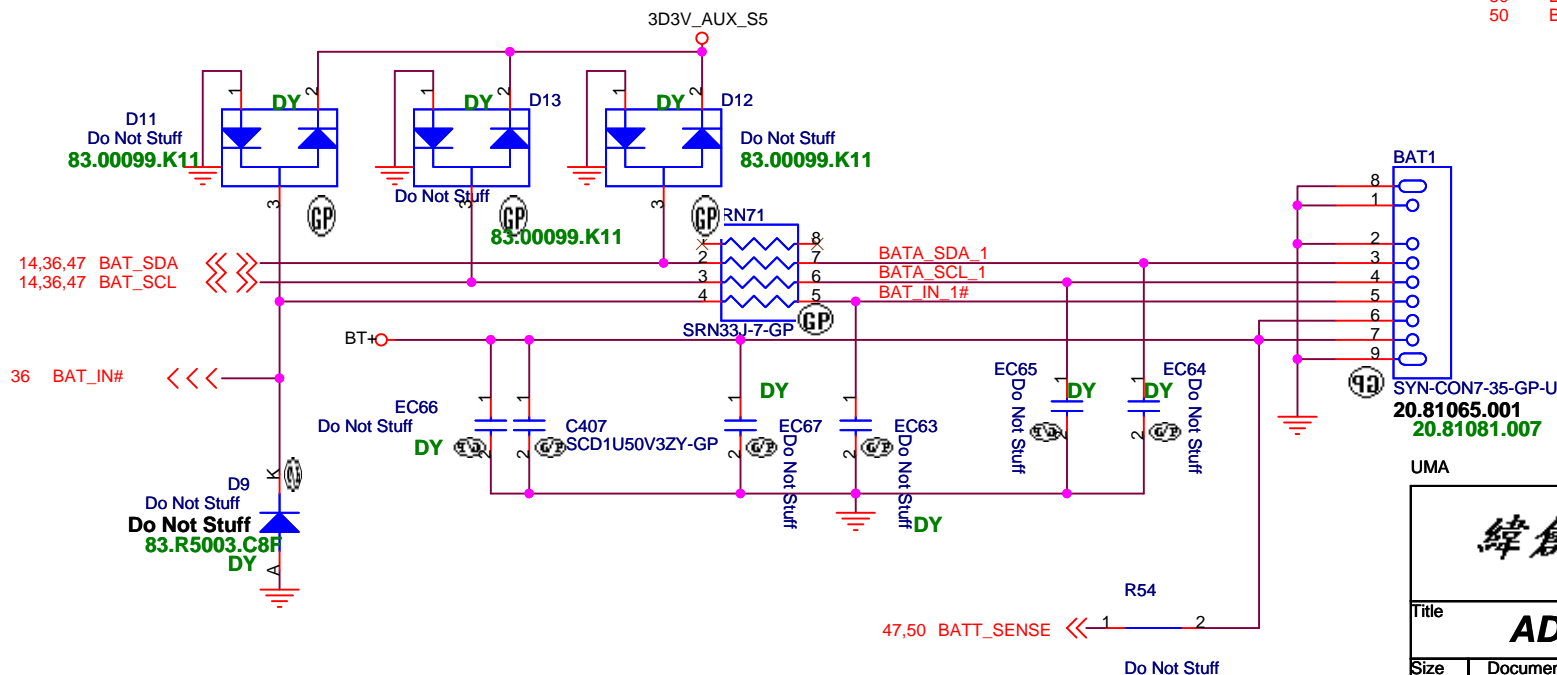
$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode







BATTERY CONNECTOR



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Title **AD/BATT CONN**

Size	Document Number
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Big Bear 2

Rev
-1

Date: Wednesday, October 22, 2008

Sheet	48	of	50
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STAND OFF

SPRING ON BOTTOM

CPU & NB

MDC

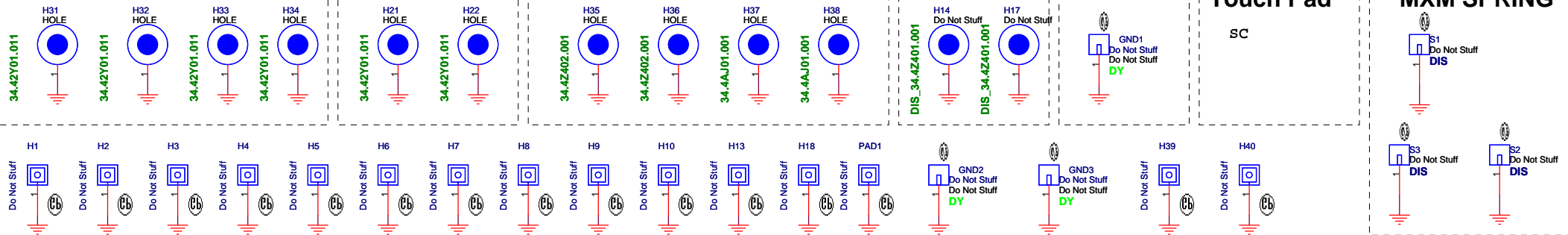
Mini Card

MXM

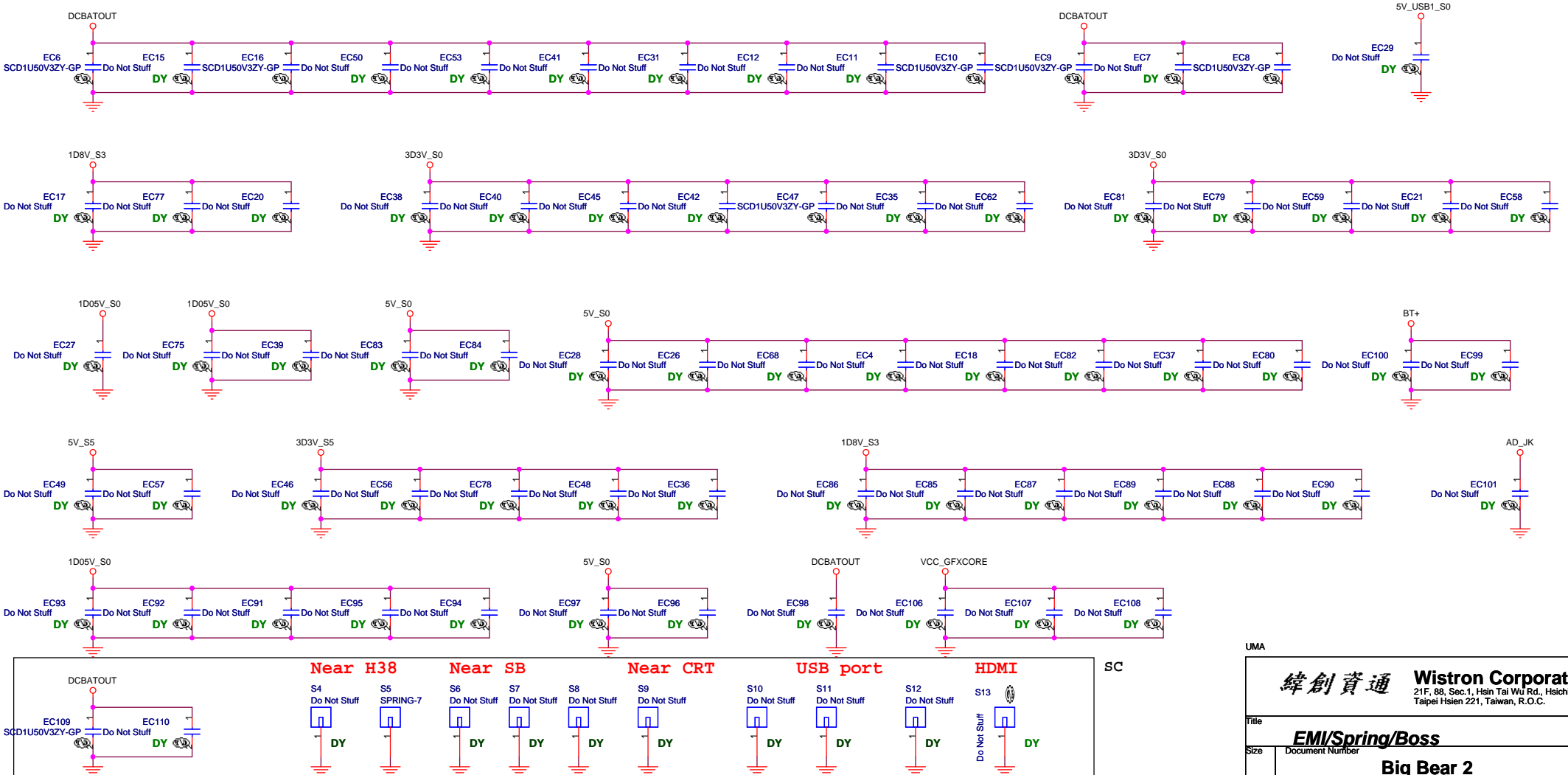
DIMM

Touch Pad

MXM SPRING

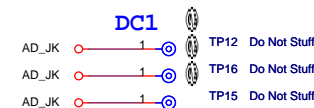
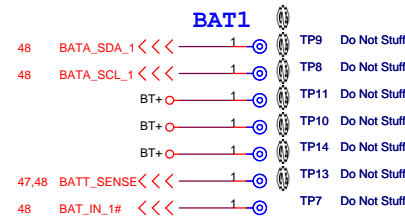
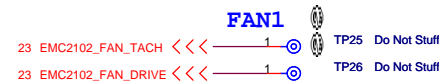
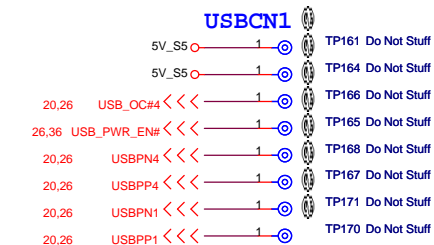
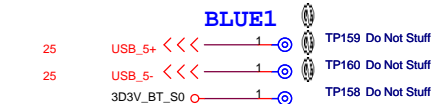
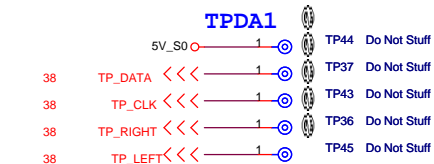
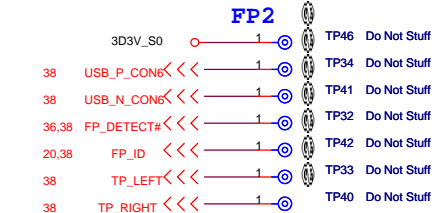
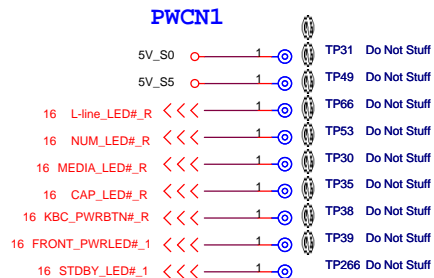
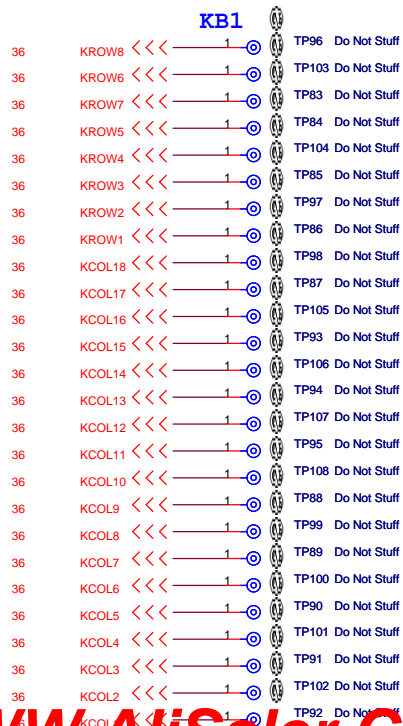
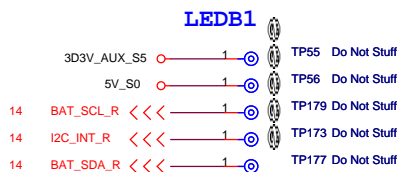
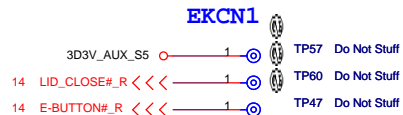
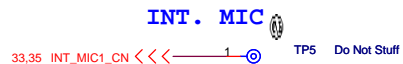
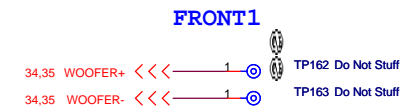
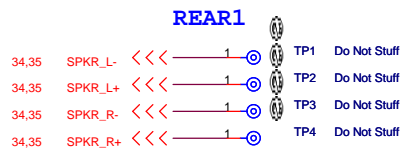


EMI



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Size	Document Number	Rev	
A3		-1	
Date: Wednesday, October 22, 2008		Sheet	50 of 51

Big Bear 2 Schematic EC Tracking Record LAB 0911 , 2008

EC #/ Page / Description / Part Affected

- EC SC01/20/Change R316 to 20R2F(For USB eye diagram)
- EC SC02/24/Swap net SATA_RXN5 SATA_RXP5
- EC SC03/29/Add C679 C680 for XF1(For IEEE common voltage channel D fail)
- EC SC04/33/Add RN95 RN104(vendor realtek request)
- EC SC05/36/Swap KBI1 pin definition